COLLOQUIUM

Center for Embedded Computer Systems

Presents

The ADRES & DRESC dynamically reconfigurable architecture and ANSI C compiler

Dr. Bjorn De Sutter
IMEC Research Labs, Belgium

Abstract

VLIW DSP architectures and their supporting compiler techniques do not scale to much more than 8 issue slots. As such they cannot offer high performance at low power consumption. To meet the performance and requirements of modern mobile applications, architectures based on coarse-grained reconfigurable arrays have been developed that overcome the limitations of VLIW DSPs. In this talk, the ADRES architecture template is presented, together with the DRESC tool chain that supports both HW synthesis of architecture instances and retargetable compilation of applications programmed in ANSI C. Results are presented for two different architecture instances for two application domains: video coding and software-defined radio, the latter of which will tape-out in Q4 2007.

Biography

Bjorn De Sutter obtained his PhD in computer science at the University of Ghent in Belgium in 2002. His PhD and post-doc research focused on whole-program analysis, program compaction and link-time binary rewriting. In IBM T.J. Watson research center he has been working on whole-program Java analysis together with Frank Tip. In 2005, he moved to IMEC, the Interuniversity Micro-Electronics Center, which is Europe's largest such research center. At IMEC, he leads the Architecture and Compiler Technology team. Bjorn De Sutter has published in, amongst others, TOPLAS, TECS, OOPSLA, ECOOP, and LCTES.

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CECS Host: Elaheh Bozorgzadeh, eli@ics.uci.edu
For more information contact: Melanie Kilian at (949) 824-9127

UNIVERSITY OF CALIFORNIA, IRVINE