

# CECS COLLOQUIUM

## Center for Embedded Computer Systems

*Presents*

### **Transparent Acceleration of Data Dependent Instructions for General Purpose Processors**

**Prof. Luigi Carro**  
**Federal University of Rio Grande do Sul**

Although transistor scaling keeps following Moore's law, and more area is available for designers, the clock frequency and ILP rate do not grow in the same rate. This way, new architectural alternatives are necessary. Reconfigurable fabric appears to be one emerging possibility: besides exploiting the parallelism among instructions, it can also accelerate sequences of data dependent code. However, coarse grain reconfiguration wide spread usage is still withheld by the need of special tools and compilers, which clearly do not sustain the reuse of legacy code without any modification. Based on all these facts, a new Binary Translation algorithm, implemented in hardware and working in parallel to the processor, responsible for transforming sequences of instructions at run-time to be executed on a dynamic coarse-grain reconfigurable array, tightly coupled to a traditional RISC machine has been proposed.

*Luigi Carro received the Electrical Engineering and the MSc degrees from Universidade Federal do Rio Grande do Sul (UFRGS), Brazil, in 1985 and 1989, respectively. From 1989 to 1991 he worked at ST-Microelectronics, Agrate, Italy, in the R&D group. In 1996 he received the doctoral degree in Computer Science from Universidade Federal do Rio Grande do Sul (UFRGS), Brazil. He is presently associate professor at the Institute of Informatics of UFRGS. His primary research interests include embedded systems design, validation, automation and test, fault tolerance for future technologies, and rapid system prototyping. He is the author of the book Digital Systems Design and Prototyping (2001, in Portuguese) and co-author of Fault-Tolerance Techniques for SRAM-based FPGAs.*

### **Adaptive Mechanisms for Meeting Energy and Real-Time Constraints in MPSoC Platforms**

**Prof. Flavio R. Wagner**  
**Federal University of Rio Grande do Sul**

MPSoC platforms for embedded, portable applications have strict requirements regarding energy constraints. In current devices, the system workload is not known at design time anymore, since users may launch different applications dynamically. Besides, many embedded applications exhibit real-time behavior. This talk will discuss run-time, adaptive mechanisms for meeting energy and real-time constraints in MPSoC platforms, including task allocation and task migration strategies, combined with dynamic voltage scaling and power management. These mechanisms are being integrated in a middleware for an MPSoC platform under development at the UFRGS, which offers a high-level, object-oriented API for application development and make adaptive mechanisms transparent to the application designer.

*Flavio R. Wagner is professor and current Director of the Institute of Informatics of the Federal University of Rio Grande do Sul (UFRGS), in Porto Alegre, Brazil. He was Chairman of the IFIP Working Group 10.5 from 2001 to 2006 and has been President of the Brazilian Computer Society. He holds a doctoral degree in Computer Engineering from the University of Kaiserslautern, in Germany, in 1983. His main research interest is the high-level co-design of the architecture and software of MPSoC-based embedded systems.*

**Tuesday, May 29, 2007**

Calit2 Auditorium

Talks begin at 11AM; Refreshments at 10:30AM

CECS Host: Professor Nikil Dutt, [dutt@ics.uci.edu](mailto:dutt@ics.uci.edu)

For more information, contact Melanie Sanders at (949) 824-1546

UNIVERSITY OF CALIFORNIA, IRVINE