

COLLOQUIUM

Center for Embedded Computer Systems

Presents

Arithmetic Optimizations for System Design

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Abstract

Arithmetic computations are the major components of the latency, complexity and power consumption of DSP systems. Careful optimization of arithmetic computations can help achieve lower power consumption, higher performance, and smaller area. Unfortunately, system designers have limited tools for optimizing these arithmetic computations. In most cases, designers rely on hand optimized library routines (for software) or IP blocks (for hardware) to implement these computations.

In this talk Dr. Fallah will present advanced algorithms for optimizing polynomials and linear systems which can achieve significantly better results compared to previously proposed techniques. The techniques can be used in a hardware design flow or before software compilation.

Biography

Farzan Fallah received the B.S. degree in electrical engineering from Sharif University of Technology, Tehran, Iran, in 1992, and the M.S. and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology, Cambridge, in 1996 and 1999, respectively. In April 1999, he joined Fujitsu Laboratories of America, where he is currently the leader of the lowpower design project. He has authored and coauthored over 40 papers. His primary research interests include low-power design and verification. Dr. Fallah is a member of the Association for Computing Machinery and the IEEE Management Society. He has served on the technical program committee of DATE, HLDVT, ISQED, and the Ph.D. Forum at DAC and has initiated the Ph.D. Forum at ASP-DAC. He has received a number of awards including a Design Automation Conference Best Paper Award and an International Conference on VLSI Design Best Paper Award.

Friday, March 9, 2007

Calit2 Auditorium

Talk begins at 3:00pm; Refreshments at 2:30pm

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