

# A Novel High Frequency, High-Efficiency, Differential Class-E Power Amplifier in 0.18 $\mu\text{m}$ CMOS

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**Abstract--** This paper presents the design of a high efficiency, low THD, 5.7GHz fully differential power amplifier for wireless communications in a standard 0.18 $\mu\text{m}$  CMOS technology. The power amplifier employs a fully differential class-E topology to achieve high power efficiency by exploiting its soft-switching property. In order to achieve high operating frequency, an injection-locked oscillator is utilized, which makes the output voltage of the power amplifier tuned at the input signal frequency. A complementary CMOS cross-coupled pair topology is employed to realize the LC-tank oscillator because it has lower phase-noise, thereby giving lower THD than the single NMOS cross-coupled pair topology. The proposed power amplifier can deliver 25dBm output power to a 50 $\Omega$  load at 5.7GHz with 42.6% power-added efficiency (PAE) from 1.8V supply voltage.

**Categories & Subject Descriptors:** B.7.1 [Integrated Circuits]: Types and Design Styles – Advanced technologies

**General Terms:** Experimentation, Design, and Measurement.

**Keywords:** Radio-Frequency Integrated Circuits, Class-E Power Amplifier, Injection-Locked, Oscillator, Phase Noise, Jitter.

## 1. INTRODUCTION

One of the most challenging building blocks in wireless RF transceivers is the power amplifier (PA). The ever-decreasing feature size of the semiconductor devices has enabled circuit designers to design compact, low cost, and low power system-on-a-chip (SOC). While the research efforts are toward the system integration, the design of an on-chip front-end power amplifier with a low total-harmonic distortion (THD) (smaller than 2%), and high power efficiency (in excess of 50%) in the mainstream CMOS technology remains a challenging problem. For the state-of-the-art applications requiring moderate-to-high output power, the PA contributes significantly to the total power consumption of the RF transceiver. The conventional power amplifier [1] cannot comply with the power consumption requirements of a low-power RF transceiver.

Recently, there have been efforts to design high frequency, high-efficiency power amplifiers. Mode-locking technique has been proposed to enable the PA working at high frequencies [2][3]. However, the locking range of a mode-locked-based power amplifier severely limits the frequency bandwidth. In addition, the driving stage of that last PA stage is a class-C preamplifier, which lowers the total power efficiency.

In this paper, we propose a fully differential class-E power amplifier incorporating an injection-locked LC tank oscillator, which is used to relax the stringent requirement on transistor sizes of the PA. The complementary CMOS cross-coupled pair topology is employed to implement the LC tank oscillator because it exhibits lower phase noise hence yielding a lower THD than the single NMOS topology. Using these techniques, the power amplifier can achieve very high operating frequency while attaining a high power-added efficiency (PAE) and a low THD.

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The remaining part of this paper is organized as follows. Section 2, gives a brief overview of the class-E power amplifier. This follows the detailed description of our proposed PA circuit. Section 3 provides the experimental results and the layout of the circuit. Finally, Section 4 presents the conclusions of our paper.

## 2. CIRCUIT DESCRIPTION

### 2.1. Basic Operation of Class-E Power Amplifier

Fig. 1 depicts the conventional class-E power amplifier (PA). The active device in a class-E PA operates as a switch, rather than a current source, turning on and off abruptly. In principle, the voltage across the switch and the current flowing through it are never simultaneously nonzero. Therefore, ideally the switch dissipates no power, and the DC supply voltage is delivered to the RF output. This concept is commonly referred to as “soft switching”. To satisfy the conditions for soft switching, the matching network components consisting of  $L$  and  $C$ , have to be calculated for a certain nominal load  $R$  seen at the input terminal of transformation network [4], i.e.,

$$L = \frac{1.15R}{\omega_c} \quad (1)$$

$$C = \frac{0.1836}{\omega_c \cdot R} \quad (2)$$

The soft switching nature of a class-E amplifier ensures that the MOS transistor is in the triode region when the switch is on, and hence acts as a simple resistor. Since the transistor has a finite resistance when it is switched on, there will be a power loss across the transistor. The power efficiency is thus equal to:

$$\text{Power Efficiency} = \frac{P_L}{P_L + P_{tr}} \quad (3)$$

where  $P_L$  is the power transferred to the load, and  $P_{tr}$  is the power dissipated in active switching device. In Eq. (1), it is implicitly assumed that the only power loss arises from the finite resistance  $R_{on}$  of the switching transistor and the power efficiency of class-E power amplifier is solely determined by this power loss in the transistor.

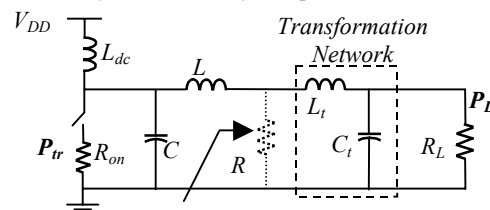


Fig. 1. Class-E power amplifier

### 2.2. Differential Class-E PA with Complementary CMOS cross-coupled pair

In RF power amplifiers, large transistor sizes are required in order to provide sufficient current to the nominal load. The situation is exacerbated as the signal frequency increases, due to the fact that the required switching current must be provided in smaller time intervals. In addition, from Eq. (3), the power loss due the finite  $R_{on}$  of the switch transistor can significantly degrade the overall power efficiency. Therefore, the size of the switching transistor is normally made as large as possible to reduce the loss due to the finite on-resistance. However, the size of the transistor cannot be made arbitrarily large due to the underlying issues.

First, the input capacitor of the switching transistor is typically tuned out by an inductive load. However, beyond a certain transistor size the inductance values required to tune out the input capacitance may become too small to be realizable. Second, a larger transistor implies larger parasitic capacitances, particularly a larger gate-drain capacitance, which causes a strong input-output coupling and hence, a potential instability.

Fig. 2 demonstrates the schematic of the proposed differential CMOS class-E power amplifier, which is designed to operate in the multi-gigahertz range of frequencies and to overcome the aforementioned obstacles.

A fully differential configuration is used to take advantage of the benefits associated with the differential architecture. First, the impact of the substrate and power/ground noise on the circuit performance is largely reduced. A differential architecture is insensitive to common-mode fluctuations, which makes it a better choice in the presence of the environmental noise sources (e.g., substrate noise, power/ground noise) than a single-ended topology, because these noise sources mostly appear as common-mode components. Moreover, since the current flowing through power transistor pair M1-M2 is charged to ground during the positive and negative half cycle respectively, there is current charged to ground twice per cycle, reducing the substrate-induced interference. Furthermore, a differential PA exhibits an odd-symmetry. As a consequence, due to the absence of the even harmonics, it shows a much better THD than the single-ended counterpart.

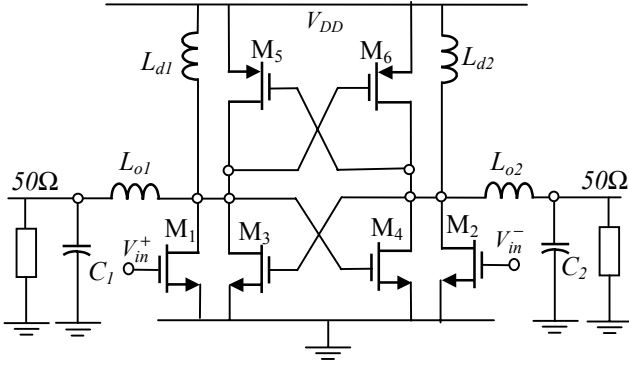


Fig. 2. The proposed differential class-E power amplifier with complementary CMOS cross-pair

In the differential configuration, the current passing through each switch is lower than that in its single-ended counterpart. This allows a smaller transistor to be used on each side of the differential pair. However, the differential configuration alone doesn't provide sufficient size reduction. In the proposed design, an injection-locked LC tank oscillator consisting of complementary cross-coupled pair M3-M6 (*cf.* Fig. 2) is utilized to solve this problem. The complementary CMOS cross-coupled pair is employed to produce the negative resistance and thus compensate the inductor loss. The LC tank oscillator tuned at the input frequency is connected to the output of the power amplifier. This causes the output of the power amplifier to run at the input frequency, resulting in a substantial reduction in the sizing requirements on the input transistors. The power amplifier with the complementary CMOS cross-coupled pair can achieve high operating frequency of 5.7GHz.

The half-circuit equivalent circuit model of the LC tank oscillator [6] connected to the output of the power amplifier is shown in Fig. 3.

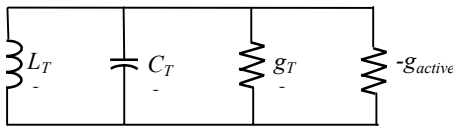


Fig. 3. The equivalent circuit of the LC tank oscillator composed of complementary CMOS cross-coupled pair

$$g_{active} = g_{m34} + g_{m56}$$

$$g_T = g_{o12} + g_{o34} + g_{o56} + 1/R_p + R_s / (L\omega)^2$$

$$L_T = L_{d1,2}$$

$$C_T = C_{PMOS} + C_{NMOS} + C_s + C_p$$

$$C_{NMOS} = C_{gs,34} + C_{db,12} + C_{db,34} + 2(C_{gd,12} + C_{gd,34})$$

$$C_{PMOS} = C_{gs,56} + C_{db,56} + 2C_{gd,56}$$

where  $R_s$ ,  $R_p$  and  $C_s$ ,  $C_p$  represents the parasitics of the symmetric spiral inductor model [7] of  $L_{d1,2}$  shown in Fig. 4.

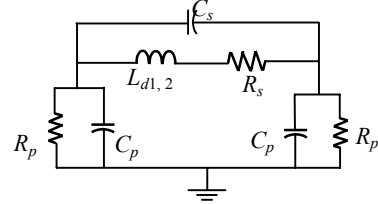


Fig. 4. Symmetric spiral inductor model of  $L_{d1,2}$

By tuning the LC tank parameters, the oscillator is tuned at the input frequency. As a consequence, it makes the output operate at the input signal frequency. This significantly reduces the current drive requirement of the power transistors; therefore, large transistor sizes are not required. The LC tank oscillator connected to the output enables the power amplifier to properly operate at very high frequencies without the requirement of large transistors. In addition, the negative conductance of the complementary CMOS cross-coupled pair helps cancel the power loss of the inductor  $L_{d1,2}$ .

The parameters of the matching networks of the proposed circuit are properly tuned. A series LC matching network is used as the input matching that matches the input impedance of the PA to 50Ω source resistance. At the output of the PA, equations (1) and (2) are realized to ensure that the voltage across the switch transistors M1-M2 and the current flowing through these transistors are never simultaneously nonzero. To achieve an output power as high as 25-30dBm with low supply voltage levels, the load impedance must be reduced. The downward LC impedance transformer (depicted in Fig. 1) composed of  $L_t$  and  $C_t$  has been used to transform the 50Ω resistor to small resistance  $R$ , where

$$R = \frac{L_t}{C_t R_L} \quad (4)$$

In the proposed PA circuit, the two inductors  $L$  and  $L_t$  in Fig. 1 are combined to give inductors  $L_{o1,2}$  in Fig. 2. Also, the grounded capacitor  $C$  in Fig. 1 includes the drain junction capacitance of transistors M1-M6 in Fig. 2.  $C_t$  in Fig. 1 is realized using capacitors  $C_{1,2}$  in Fig. 2. Fig. 5 depicts the simulated drain voltage and current waveforms of the input power transistor M1. The waveforms confirm the switching mode behavior of the proposed design, a condition that is necessary for the class-E operation of the amplifier and guarantees the small power loss on the switch, hence the high efficiency.

Another issue regarding the power amplifier is the total harmonic distortion (THD). Although the use of the injection locked oscillator enables the power amplifier to operate at high frequencies, the phase noise of the LC tank oscillator introduces some harmonics, which increases the THD of the power amplifier. In fact, a detailed large-signal analysis of the injection-locked PA given in Appendix I proves that the THD of the PA is lowered by reducing the phase noise. It has been experimentally proven that the oscillator using complementary CMOS cross-coupled pair topology has lower phase noise compared to NMOS cross-coupled configuration due to its symmetrical properties [8]. Therefore, the complementary CMOS cross-coupled pair topology is employed to realize the LC-tank oscillator because it has lower phase-noise, thereby giving lower THD than the single NMOS topology. Post-layout simulations confirm this conclusion. At 5.7GHz, the simulated THD of the power amplifier with complementary CMOS

cross-coupled pair topology is 1.41%, compared to the simulated THD of 3.21% achieved using NMOS cross-coupled pair topology. This gives us more than 2X improvement for the linearity of the class-E power amplifier.

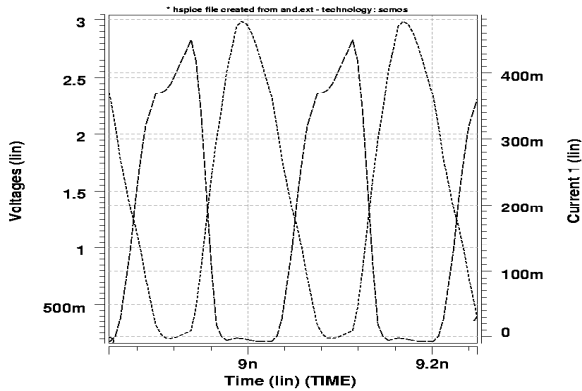


Fig. 5. Simulated waveforms of the input transistor M1 shown in Fig. 2.

### 3. EXPERIMENTAL RESULTS

The proposed differential class-E power amplifier is simulated using HSPICE and Cadence. The layout of the proposed PA is shown in Fig. 6. Fig. 7 shows the output power and power added efficiency (PAE) vs. the supply voltage variation. When changing the supply voltage from 1V to 2.1V, the output power changes approximately proportional to  $V_{DD}^2$  from 112mW to 426mW. Notice that the PAE remains close to its maximum value for supply voltage of 1.8V. The reduction in the PAE for low values of the output power is partly due to the low-valued constant input power being applied to the amplifier. Fig. 8 shows how the output power and PAE change, as a function of the input frequency. The maximum PAE of 42.6% is achieved at 5.7GHz. The spectrum of the output power is depicted in Fig. 9.

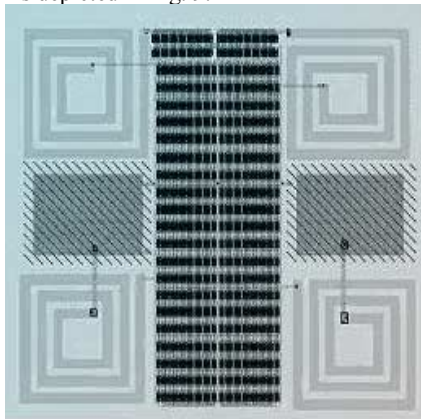


Fig. 6. Layout of designed differential class-E power amplifier

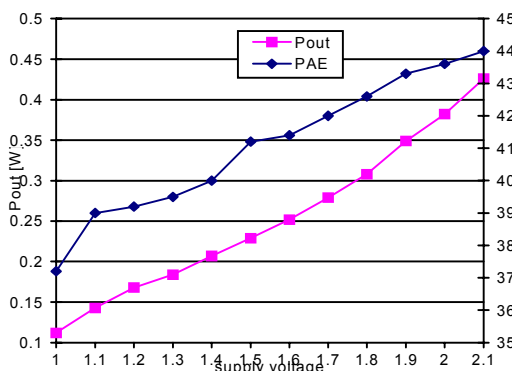


Fig. 7. Output power and PAE vs. supply voltage @ 5.7GHz

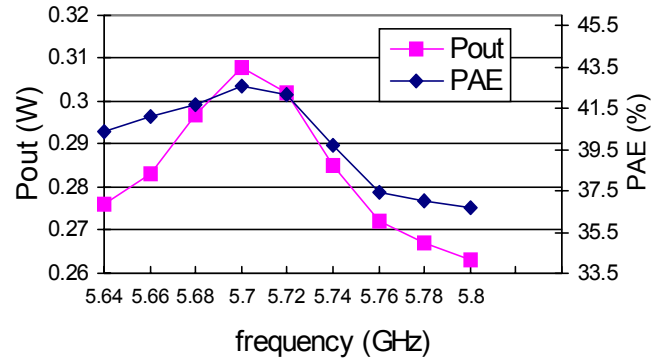


Fig. 8. Output power and PAE vs. frequency

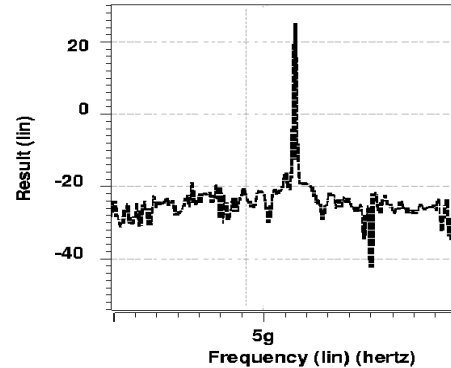


Fig. 9. The spectrum of the output power of the proposed class-E power amplifier

After designing the layout of the circuit (presented in Fig. 6), a post-layout simulation is performed on circuit for all the process design corners. Table 1 compares the performance of the proposed PA with the recently published CMOS class-E power amplifiers. As can be seen from Table 1, our proposed PA circuit achieves higher power efficiency at higher signal frequency compared to the previously proposed class-E PA circuits.

Table 1: Performance comparison between the proposed PA and the PAs presented in [2], [3], and [4].

Ref.	Tech.	freq.	$V_{DD}$	$P_{out}$	PAE
[2]	0.35 $\mu$ m	700MHz	2.2V	29.5dBm	62%
[3]	0.35 $\mu$ m	1.9GHz	2V	30dBm	48%
[5]	0.25 $\mu$ m	900MHz	1.8V	29.5dBm	41%
This work	0.18 $\mu$ m	5.7GHz	1.8V	25dBm	42.6%

### 4. CONCLUSIONS

A differential class-E power amplifier was proposed in this paper. Complementary CMOS cross-coupled pair topology was employed as an oscillator because it has lower phase-noise, thereby giving lower THD than the single NMOS topology. The proposed power amplifier can deliver 25dBm output power to a 50 $\Omega$  load at 5.7GHz with 42.6% power-added efficiency (PAE) from 1.8V supply.

### APPENDIX I

The proposed power amplifier employs an injection-locked LC oscillator. Like any oscillator circuit, the incorporated oscillator is susceptible to random variations in the zero crossing points from their ideal position along the time axis. This random variation of the phase is called phase noise. Suppose that the input waveform to the PA circuit in Fig. 2 is a periodic sinusoidal signal:

$$V_g(t) = B \sin \omega_{in} t \quad (6)$$

The single-ended voltage across the drain of each MOS transistor, M1 and M2, is subject to small random phase variation  $\Phi_n(t)$ , i.e.,

$$V_d(t) = A \cos[\omega_{in} t + \Phi_n(t)] \quad (7)$$

If  $|\Phi_n(t)| \ll 1 \text{ rad}$ , we have:

$$V_d(t) = A \cos(\omega_{in} t) - A \Phi_n(t) \sin(\omega_{in} t) \quad (8)$$

In the frequency domain, the presence of the phase-noise in the oscillator causes a deviation from an impulse function. In fact, the spectrum exhibits skirt around the center frequency,  $\omega_{in}$ .

The soft switching nature of a class-E power amplifier ensures that the MOS transistor is in the triode region when the switch is on. Using short-channel I-V relationship for the MOS transistors [9], M1 and M2 in Fig. 2, while accounting for the mobility degradation, the drain current is characterized as follows:

$$I_{D1}(t) = \mu_n C_{ox} \frac{W \{ [V_{gs}(t) - V_T] V_d - 0.5(1 + \delta) V_d^2 \}}{L \{ 1 + \theta [V_{gs}(t) - V_T] \} (1 + \frac{V_d}{LE_c})} \quad (9)$$

$$= \frac{\mu_n C_{ox} W}{L(1 + \frac{V_d}{LE_c})} \cdot \frac{\{ [V_{gs0}(t) - V_T] V_d - 0.5(1 + \delta) V_d^2 + V_d V_g(t) \}}{\{ 1 + \theta (V_{gs0} - V_T) + \theta V_g(t) \}}$$

Where  $V_{gs0}$  is the DC component of the input signal and  $V_g(t)$  is the AC component. The critical electric field before the on-set of velocity saturation is represented by  $E_c$ . To simplify the calculation, we first define  $I_{D0}$  to be:

$$I_{D0}(t) = \mu_n C_{ox} \frac{W \{ [V_{gs0} - V_T] V_d - 0.5(1 + \delta) V_d^2 \}}{L \{ 1 + \theta [V_{gs0} - V_T] \} (1 + \frac{V_d}{LE_c})}$$

Let:

$$a = \frac{\mu_n C_{ox} W [V_{gs0} - V_T]}{L [1 + \theta (V_{gs0} - V_T)]}$$

$$b = \frac{1}{LE_c}$$

$$c = \frac{0.5(1 + \delta)}{V_{gs0} - V_T}$$

We have:

$$I_{D0} = a(V_d - V_d^2)(1 - bV_d + b^2V_d^2) \quad (10)$$

$$= a[V_d - (b + c)V_d^2 + b(b + c)V_d^3]$$

$$= a(V_d - dV_d^2 + bV_d^3)$$

where  $d = b + c$ . Also, define

$$\alpha = \frac{\theta}{1 + \theta [V_{gs0} - V_T]} \quad (11)$$

The power transistors M1 and M2 are in the triode region when they turn on, thereby the drain voltage  $V_d$  is small. Therefore, one can assume that  $|V_d| < LE_c$ , and  $|cV_d| < 1$ . This leads to the following:

$$\beta = \frac{1}{[V_{gs0} - V_T] - 0.5(1 + \delta)V_d}$$

$$= e \frac{1}{1 - cV_d} \approx e(1 + cV_d + c^2V_d^2) + O(V_d^k) \quad (12)$$

where  $e = 1/(V_{gs0} - V_T)$ . Using the new simplified expressions defined above, the drain current  $I_D$  is obtained as follows:

$$I_{D1} = I_{D0} \frac{1 + \beta V_g(t)}{1 + \alpha V_g(t)} \quad (13)$$

$$= I_{D0} [1 + \beta V_g(t)] [1 - \alpha V_g(t) + \alpha^2 V_g^2(t) \Lambda]$$

Substituting (10), (11), and (12) in (13), yields the following expression for the drain current  $I_{D1}$  of the power transistor M1:

$$I_{D1} = A [V_d + (e - \alpha) V_g V_d + (ec + \alpha d - de) V_d^2 V_g + (\alpha - \alpha e) V_g^2 V_d - d V_d^2 + b d V_d^3]$$

Similar to any differential architecture, the proposed PA circuit has odd symmetry. Therefore, even harmonics are absent in the differential output current,

$$\Delta I_D = I_{D1} - I_{D2} \quad (14)$$

$$= 2a [V_d + g V_g V_d^2 + h V_g^2 V_d - k V_d^3]$$

where  $g = ec + \alpha d - de$  and  $h = \alpha(1 - e)$ , and  $k = bd$ . Plugging equations (6) and (7) in Eq. (14), the third-order harmonic of the differential current is readily obtained:

$$HD_3 \approx ABg \left[ \frac{1}{4} - \frac{1}{4} \Phi_n^2(t) + \frac{1}{2} \Phi_n(t) \right] + B^2 h \left[ -\frac{1}{4} + \frac{1}{4} \Phi_n(t) \right] \quad (15)$$

$$- A^2 k \left[ \frac{1}{4} - \frac{1}{4} \Phi_n^3(t) - \frac{3}{4} \Phi_n(t) + \frac{3}{4} \Phi_n^2(t) \right]$$

$$= -\frac{A^2 k}{4} [1 - \Phi_n(t)]^3 + \frac{ABg}{4} [2 - (1 - \Phi_n(t))^2] - \frac{B^2 h}{4} [1 - \Phi_n(t)]$$

The third-order harmonic  $HD_3$  attains its minimum value at  $\Phi_n(t) = 0$ , and is a monotonically increasing function of the phase noise,  $\Phi_n(t)$ . Since the second harmonic distortion can be suppressed in the differential configuration, a low  $HD_3$  will enable us to achieve a low THD for the power amplifier.

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