

1D-19 : Design and Implementation of a Duplex AMBA-TMS Transducer

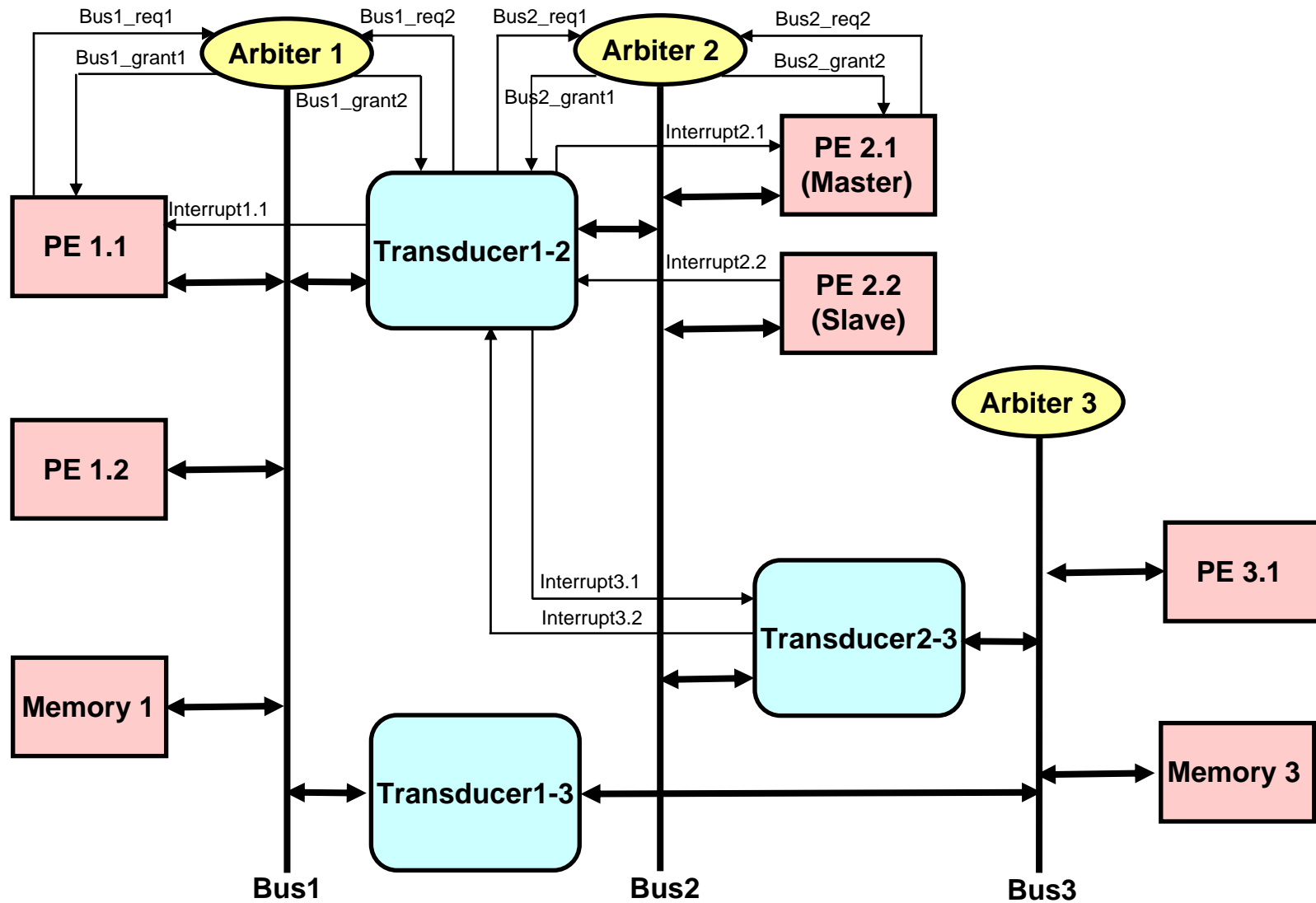
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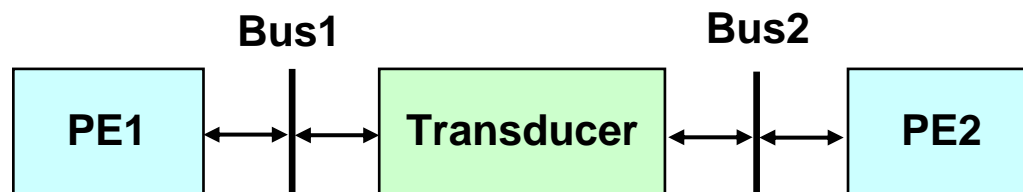


General System Model



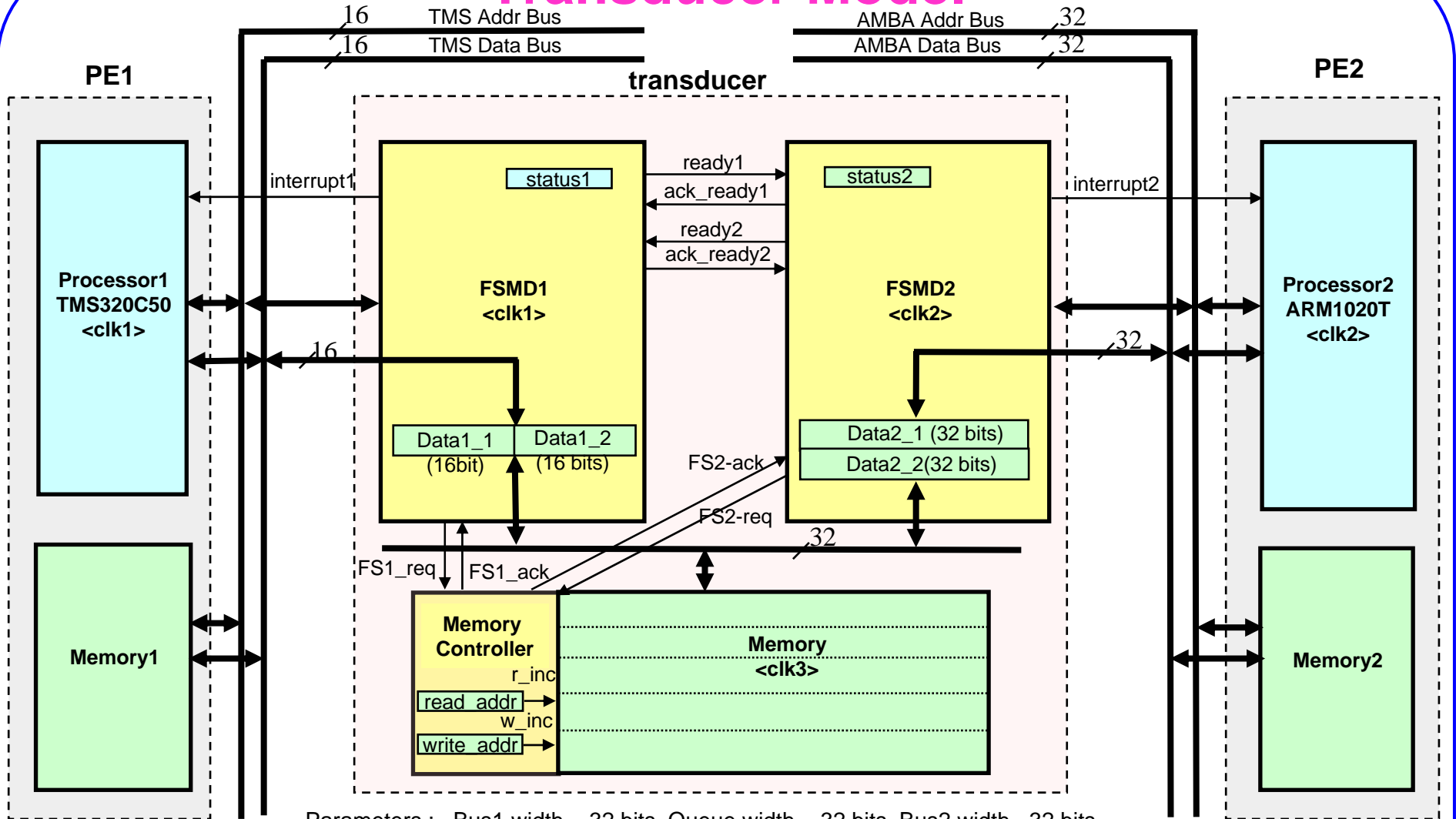
Problems

- **Different cores in system may have incompatible interface**
 - Different clock speed
 - Different control signals
 - Incompatible ports
- **Need interface logic (transducer)**
 - Translates between protocols of Bus1 and Bus2



- **Need synthesis algorithm for transducer generation**

Transducer Model



Parameters : Bus1 width = 32 bits, Queue width = 32 bits, Bus2 width = 32 bits
 sBus1 = TMS320C5X
 Bus2 = AMBA
 PE1 = Dummy custom processor (even parity checker)
 PE2 = Dummy ARM1020E (one's counter)
 clk(clk1 = 50 Mhz, clk2 = 70 Mhz, clk3 = 30 Mhz)
 FIFO Memory = Synchronous SRAM
 Status bits : FSMD1_ Ready, Data2_ Ready, Q_ Full

Conclusions

- **Results**

- Implemented a transducer for TMS and AMBA protocols
- Demonstrated a working transducer on FPGA

- **Benefits**

- Bus protocol to bus protocol translation
- IP protocol to bus protocol translation

- **Contributions**

- Provided general communication interface for multi-core systems
- One transducer for all
- Transducer generation algorithm

