A Performance and Power Analysis of WK-Recursive and Mesh Networks for Network-on-Chips

D. Rahmati[1], A. E. Kiasari[1,2], S. Hessabi[1], H. Sarbazi-Azad[1,2]
[1] Department of Computer Engineering,
Sharif University of Technology,
Tehran, Iran
[2] School of Computer Science,
Institute for Studies in theoretical Physics and Mathematics (IPM)
Tehran, Iran

***Abstract*—Network-on-Chip (NoC) has been proposed as an attractive alternative to traditional dedicated wires to achieve high performance and modularity. Power efficiency is one of the most important concerns in NoC architecture design. The choice of network topology is important in designing a low-power and high-performance NoC. In this paper, we propose the use of the WK-recursive networks to be used as the underlying topology in NoC. We have implemented VHDL hardware model of mesh and WK-recursive topologies and measured the latency results using simulation with these implementation. We also propose a novel approach in high level power modeling based on latency for these topologies and show that the power consumption of WK-recursive topology is less than that of the equivalent mesh on a chip.**

***Index Terms*—System-on-chips, Network-on-chips, Mesh, WK-Recursive mesh, Routing, Power, Performance.**

I. INTRODUCTION

With the advance of the semiconductor technology, the enormous number of transistors available on a single chip allows designers to integrate dozens of IP (Intellectual Property) blocks together with large amounts of embedded memory. Such IPs can be CPU or DSP cores, video stream processors, high-bandwidth I/O, *etc*. Shared-medium busses do not scale well, and do not fully utilize potentially available bandwidth. As the feature sizes shrink, and the overall chip size relatively increases, the interconnects start behaving as lossy transmission lines. Line delays have become
very long as compared to gate delays causing synchronization problems between cores. A significant amount of power is dissipated on long interconnects and in clocking network. This trend only worsens as the clock frequencies increase and the features sizes decrease. Lowering the power supply voltage and designing low swing circuits decrease the overall power consumption at the cost of higher data errors.

One solution to these problems is to treat systems on a chip implemented using *micro-networks*, or *Networks on Chips* (NoCs). Networks have a much higher bandwidth due to multiple concurrent connections. Regularity enables design modularity, which in turn provides a standard interface for easier component reuse and better interoperability. Overall performance and scalability increase since the networking resources are shared. Scheduling of traffic on shared resources prevents latency increases on critical signals.

Power efficiency is one of the most important concerns in NoC architecture design. Consider a 10×10 tile-based NoC, assuming a regular mesh topology and 32 bit link width in 0.18*um* technology and minimal spacing, under 100Mbit/s pair-wise communication demands, interconnects will dissipate 290W of power [4]. Thus, reducing the power consumption on global interconnects is a key factor to the success of NoC designs.

The choice of network topology is important in designing a low-power NoC. Different NoC topologies can dramatically affect the network characteristics, such as average inter-IP distance, total wire length, and communication flow distributions. These characteristics in turn determine the power efficiency of NoC architectures. In recent years, several new parallel computer architectures have been proposed in the literature for building massively parallel computer systems to increase computation speed. A major drawback for these networks is that there are not predefined modules existent for them when they are fabricated onto a monolithic chip. The reason is that they are not truly expansible. In addition, the irregularity of node degrees also makes them costly for VLSI implementation.

The WK-recursive networks [7] are a class of recursively scalable networks with many desirable properties. They offer a high degree of regularity, scalability, and symmetry, which very well conform to a modular design and implementation of distributed systems involving a large number of computing elements. In [7], a VLSI implementation of the WK-recursive networks is described, and a routing algorithm is developed. This algorithm defines the physical channels which must be traversed, but does not address the use of virtual channels. Virtual channels are usually used to increase performance and to design deadlock free routing algorithms. In this paper we propose a new virtual channel selection policy for WK-recursive network which results in a deadlock-free routing algorithm.

In this research, we compare the two most important performance factors (latency and power) of the same size mesh and WK-recursive networks for NoC implementation. To this end, we have implemented a hardware model using VHDL for accurate simulation of the networks in question. A routing algorithm for the WK-recursive network has been proposed and the performance of the two networks under similar working conditions has been assessed and compared. We also develop a high level power consumption model to compare the candidate networks with their energy requirements.

II. WK-RECURSIVE NETWORK STRUCTURE

The WK-recursive networks can be constructed recursively by grouping basic modules. Any d-node complete graph can serve as the basic module. Throughout this paper, we use WK(d,t) to denote a WK-recursive network of level t whose basic modules are some d-node complete graph, where $d > 1$ and $t \geq 1$. Each node of WK(d,t) is uniquely identified by a sequence of t numbers, and each of its edges is represented by a pair of nodes. We define WK(d,t) formally as follows:

Definition 2.1. The node set of WK(d,t) is denoted by $\{a_t a_{t-1} \ldots a_2 a_1 | a_i \in [0,d\text{-}1]$ for $1 \leq i \leq t\}$. The adjacency is defined as follows: $a_t a_{t-1} \ldots a_2 a_1$ is adjacent to (1) $a_t a_{t-1} \ldots a_2 b$ where $0 \leq b \leq d$ - 1 and $b \neq a_1$, and (2) $a_t a_{t-1} \cdots a_{i+1} a_{i-1} (a_i)^{i-1}$ if $a_i \neq a_{i-1}$ and $a_{i-1} = a_{i-2} = \ldots = a_2 = a_1$, where $(a_i)^{i-1}$ represents i -1 consecutive a_i's. Besides, an *open edge* is incident to $a_t a_{t-1} \ldots a_2 a_1$ if $a_l = \ldots = a_2 = a_1$. Each edge of WK(d,t) is assigned a label as follows: 0 if it is of type(1), i - 1 if it is of type (2), and t if it is an open edge. The edges of type (1) are referred to as *substituting edges,* and the edges of type (2) are referred to as *flipping edges.*

In Fig. 1, the topologies of 16-node WK(4,2) and mesh(4x4) are shown. In WK(d,t), each node is of degree d, and there are totally d^t nodes and $d + d(d^t - 1) / 2$ edges. In [2], it has been shown that the diameter of WK(d,t) depends on d and equal to 2^t -1.

Definition 2.2. For any two nodes U and V in WK(d,t), we define $U =_i V$ if they belong to the same subnetwork of level i in WK(d,t), and $U \neq_i V$ if they belong to two distinct subnetworks of level i in *WK(d,t)*.

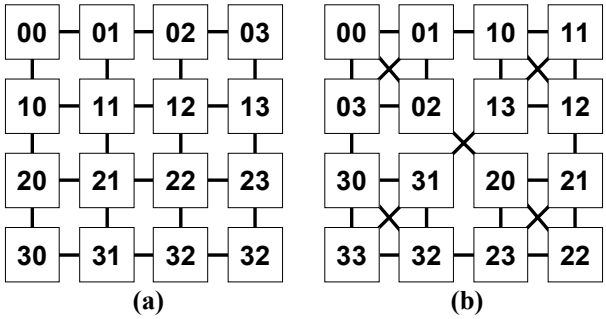


Fig. 1. The topologies of (a) Mesh(4x4) and (b) WK(4,2) with 16 nodes.

Definition 2.3. For each i, $1 \leq i \leq t$, a node $S = a_t a_{t-1} \ldots a_2 a_1$ in WK(d,t) is called an *i-frontier,* if $S = a_t a_{t-1} \ldots a_{i+1} (a_i)^i$.

Remarks. Two nodes connected by a flipping edge of label i are i-frontiers. Also, by definition, if a node is an i-frontier, it is also a j-frontier for $1 \leq j < i$.

A. Routing algorithms

Each wormhole routing algorithm includes two important parts: (1) physical channel selection rule and (2) virtual channel selection rule. Physical channel selection rule chooses the next physical channel to route the message and virtual channel selection rule chooses the proper virtual channel in selected physical channel by considering of deadlock avoidance conditions.

B. Physical channel selection rule

Suppose S and T are the source node and destination node in WK(d,t), respectively. A routing path between them can be constructed as follows [1].

$S \neq_{i-1} T$. This can be easily done by examining the identifiers of S and T from the left, and finding the first position where they differ.

Step 2. Determine the flipping edge, say (W,X), such that $S \neq_{i-1} W$ and $X \neq_{i-1} T$. The flipping edge is the bridge between the two sub-networks of level i-1 where S and T reside. The nodes W and X are (i-1)-frontiers, and they can uniquely be determined by examining the identifiers of S and T.

Step 3. Determine the routing path from S to W, and the routing path from X to T, recursively. The routing path from S to T is the concatenation of the routing path from S to W, the flipping edge (W,X), and the routing path from X to T.

C. Virtual channel selection rule

After selection of next physical channel according to the algorithm in previous section, suitable virtual channel must be selected in this physical channel by considering deadlock avoidance conditions.

1) The Positive-hop (PHop) policy

In the PHop policy [1], a message is placed in a virtual channel of class 0 in the source node upon injection into the network. During routing, a message is placed in the virtual channel of class i in an intermediate node if it has already completed i hops. Since the maximum number of hops a message can take equals the diameter of the network, the maximum number of virtual channel classes required in each node equals the diameter of the network; for WK(d,t), this number equals 2^t -1.

2) The Flipping-hop (FHop) policy

We now propose a novel virtual channel selection rule for WK-recursive networks which has less requirements than PHop policy. In PHop policy, the virtual channel class number is incremented in each hop but in FHop policy a message is placed in a virtual channel of class 0 in the source node and in an intermediate node, and the virtual channel class number is incremented if the selected physical channel is corresponding to a flipping edge. Since the maximum number of flipping edges in a path equals the half of diameter of the network [2], the maximum number of virtual channel classes required in each node equals the half of the diameter; for WK(d,t), this number equals 2^{t-1}.

D. Performance of PHop and FHop

To compare the performance of these routing algorithms, we have developed a VHDL based cycle accurate model for evaluating the latency and power of NoC based interconnection architectures. The design is parameterized on (i) size of packets, (ii) length and width of physical links, (iii) number and depth of virtual channels. This simulation model can be used for the WK-recursive networks of any size with wormhole switching. We compare the performances of PHop and FHop wormhole routing algorithms. We have simulated these routing algorithms for WK(4,2). Also we have considered fixed length messages of 32 flits. Nodes generate traffic independently of each other, and which follows a Poisson process. For the destination address of each message, we have considered the uniform traffic pattern.

In Fig. 2, the average message latency is plotted against message generation rate for WK(4,2) network with FHop routing algorithm and with 32-flit messages. In WK(4,2), we need 3 and 2 virtual channel classes for PHop and FHop routing algorithms and we have also used 2 and 3 virtual channels in each class, respectively. Therefore, there are 6 virtual channels per physical channel in both networks that can ensure a fair comparison under almost equal hardware cost. Also in our simulation experiments all virtual channels are of 1-flit depth. As you see in Fig. 2, for low and medium traffic loads, these routing algorithms have the same latency, but they begin to behave differently for high traffic loads and around the saturation region. The FHop routing algorithm has better performance than PHop routing algorithm. Therefore, from now on, we use the FHop routing algorithm for message routing in WK-recursive networks.

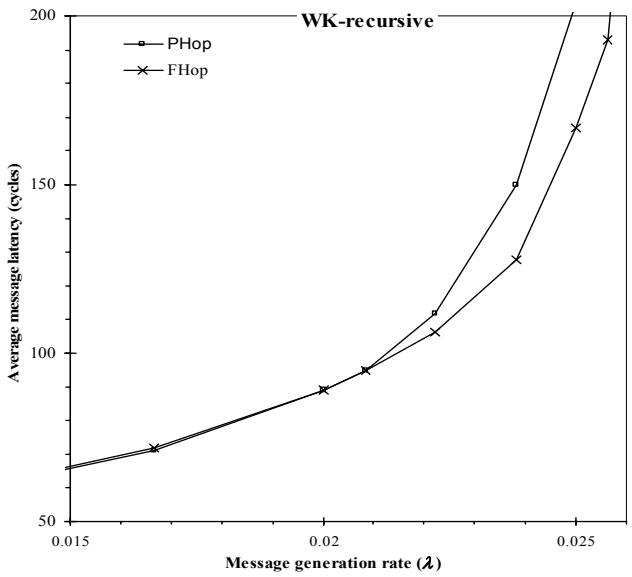


Fig. 2. Message latency in WK(4,2) with PHop and FHop routing algorithms.

III. MESH AND WK-RECURSIVE HARDWARE MODEL AND LATENCY COMPARISON

The top most shared component in this hardware model is the NoC node, in which *PE* (Processing Element) and *router* are the main components. The *PE* is a module that injects/ejects the generated/receiving packets based on a traffic model like uniform, hotspot, etc. Routers receive packets on their input channels and after routinga packet based on the routing algorithm and destination address, the packet is sent to the selected output channel. Fig. 3 shows internal structure of a *node*. A *router* consists of several different parts such as *Address Extractor* which determines and manipulates the packet headers and buffers some flits of the packet, *Multiplexer* and *De-Multiplexer* which handle the virtual channel operations, *Selector* unit which applies the virtual channel selection rule, *Crossbar switch* which directly connects each input channel to each unoccupied output channel, *Reservator* unit which controls the crossbar switch and other related sub-modules. When a specific topology like mesh or WK-recursive is supposed to be modeled by such components, a top-level wrapper module is implemented that connects several nodes of this type to each other based on the structure of the specified topology. We have simulated the hardware models of the mesh and WK-recursive networks to extract accurate quantities, e.g. latency values.

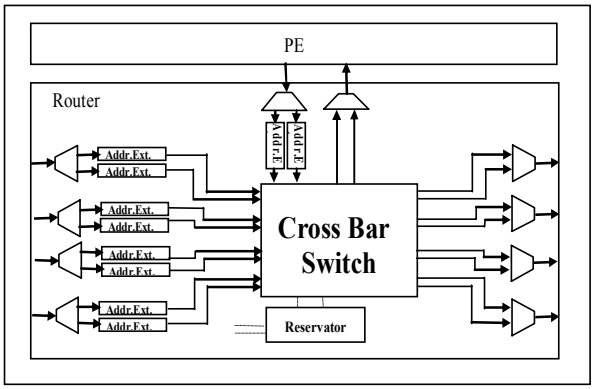


Fig. 3. Hardware implementation of a node with a PE and a Router.

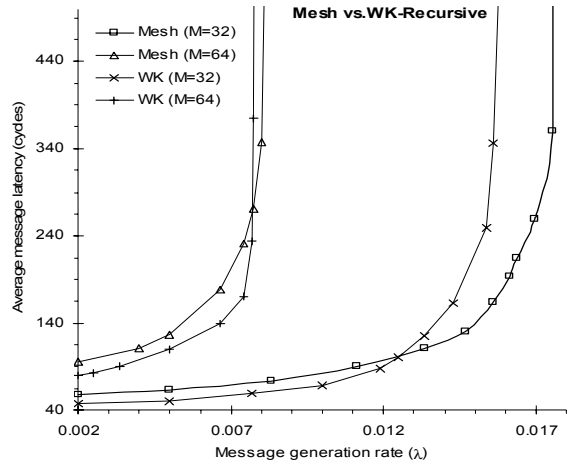
In Fig. 4, the average message latency is plotted as a function of average message generation rate at each node for a 4x4 mesh interconnection network with XY routing algorithm [3] and a WK(4,2) network with FHop routing algorithm. In WK(4,2), we need 2 virtual channel classes for FHop routing algorithm. For low traffic loads, the WK-recursive provides a better performance compared to the mesh network, but they begin to behave differently near high traffic regions. It is notable that a usual advice on using any networked system is "not take the network working near saturation region". Having considered this and also the fact that most of networks rarely enter such traffic regions, we can conclude that the WK-recursive network can outperform its equivalent mesh network when average message latency is considered.

IV. MESH AND WK-RECURSIVE POWER MODELING AND COMPARISON

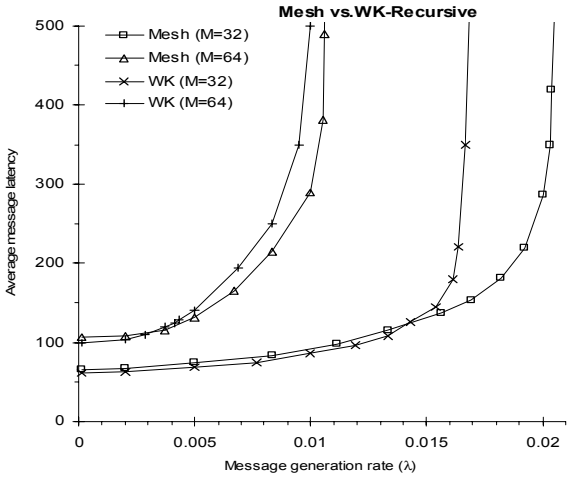
Reducing power consumption is required in today's semiconductor designs. Silicon technology advances have made it possible to pack millions of transistors switching at high clock speeds on a single chip. While these advances bring unprecedented performance to electronic products, they pose difficult power dissipation and distribution problems [5]. These problems must be addressed, because consumers demand longer battery life in addition to lower cost in computers, battery-operated systems, medical devices, telecommunications equipment and many high-volume consumer products. In this section, we propose a novel high level approach for modeling the power consumption of mesh and WK-recursive NoCs. The model computes power dissipation for a packet crossing the network, thus static and dynamic powers are both included in our analysis.

We first introduce some assumptions and definitions used in our analysis.

- The average distance of the mesh and WK-recursive networks are defined as D_{mesh} and D_{wk} .



(a)



(b)

Fig. 4. Message latency in WK(4,2) and Mesh(4x4) with (a) 2 and (b) 4 virtual channels.

- The uniform traffic pattern is used for message destination address.

- The length of wire between two switches is fixed.

- The power consumption is calculated for two different operating regions of the NoC, namely the low and high traffic regions. The low traffic region in a NoC is the region that there is no packet contention or the contention is rare. Also the high traffic is defined as a region that packet blocking is frequently occurred but there is no packet deadlock and network does not enter the saturation region. Let λ be the packet generation rate at a node and λ_s be the value of λ at the saturation point (the point from where the saturation region starts). Let the low traffic load be defined as $\lambda \leq 0.6\lambda_s$ and the high traffic region be defined as $0.6\lambda_s < \lambda < \lambda_s$.

As defined in [6][8], the average energy consumed for transferring a packet between two nodes is as follows:

E_P: Total energy dissipated for packet transfer
E_B: Energy dissipated for packet buffering
E_S: Switching energy dissipated for packet transfer
E_W: Energy dissipated in wires for packet transfer
$E_P = E_B + E_S + E_W$

We have

$$E_{BS} = E_B + E_S,\ E_P = E_{BS} + E_W \quad (1)$$

We consider both the buffering and switching (router) energy in a single parameter E_{BS}. Also we define E^C_W as average wiring energy which is dissipated between two switches for a packet transfer, $E^C_{BS,\ Low}$ is average buffering and switching energy which is dissipated in a switch for a packet transfer in low traffic and $E^C_{BS,\ High}$ for the high traffic. $E_{blocking}$ is the average blocking energy which is dissipated for a packet transfer in high traffic. This parameter represents the extra buffering energy which is dissipated in switch buffers during packet blocking. We estimate this parameter in the next section where we calculate the energy dissipation for high traffic mode of operation. At last we define

$$\alpha = E^C_W / E^C_{BS,\ Low} \quad (2)$$

in order to simplify the calculations. It shows the relation of wiring and router energy dissipation for a packet transfer.

A. Low traffic modeling

In low traffic region, packets are transferred across the network with no contention or negligible contention. Using equation (1) and (2), the average total energy dissipated for a packet transfer in the mesh and WK-recursive network topologies can be computed as:

$$E_{P,\ WK,\ Low} = (D_{WK} + 1).\ E^C_{BS,\ Low} + D_{WK}.\ E^C_W$$

and the same formula for mesh network:

$$E_{P,\ Mesh,\ Low} = (D_{Mesh} + 1).\ E^C_{BS,\ Low} + D_{Mesh}.\ E^C_W$$

Therefore, we define K as follows:

$$K = \frac{E_{P,WK,Low}}{E_{P,Mesh,Low}} = \frac{(\alpha+1)D_{WK}+1}{(\alpha+1)D_{Mesh}+1} \quad (3)$$

where α is the parameter in equation (2) and K shows the ration of the energy dissipated for Mesh and WK-recursive in low traffic region for a packet transfer. For Mesh (4x4) and WK(4,2), we have D_{WK}=2.21, D_{Mesh}=2.67 and thus

$$K = \frac{2.21\alpha + 3.21}{2.67\alpha + 3.67}$$

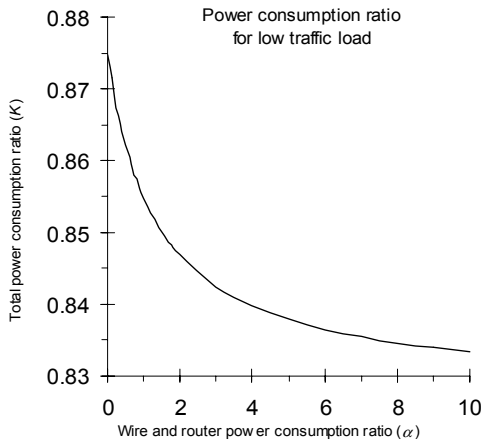


Fig. 5. The ratio of a packet transfer power dissipation for a WK(4,2) and mesh(4x4) as function of α for low traffic load.

Depending on all values of α, the power consumption ratio may vary from 0.83 to 0.88 as is shown in Fig. 5. This means that the WK-recursive consumes lower amount of energy than its mesh counterpart in low traffic.

B. High traffic modeling

Near and in high traffic regions, the energy consumption is heavily affected by the packet contention. In this case a large amount of the dissipated energy comes from packet blocking (energy consumed for buffering). The other forms of energy dissipation in wires, switching hardware, and general buffering is almost the same for low traffic load.

Let us define two parameters T_{Mesh} and T_{WK} representing the average blocking time of a packet when crossing the network. The energy dissipated for a packet transfer can be written as

$$E_{P,\ WK,\ High} = E_{P,\ WK,\ Low} + E_{blocking,\ WK}$$
$$E_{P,\ Mesh,\ High} = E_{P,\ Mesh,\ Low} + E_{blocking,\ Mesh} \quad (4)$$

also, the average energy consumed due to the message blocking is proportional to its average blocking time and also the average number of switches it traverses, i.e. $E_{blocking,\ WK} \propto T_{WK}.(D_{WK}+1)$ and $E_{blocking,\ Mesh} \propto T_{Mesh}.(D_{Mesh}+1)$. By using a constant we can write

$$E_{blocking,\ WK} = C.T_{WK}.(D_{WK}+1),$$

$$E_{blocking,\ Mesh} = C.T_{Mesh}.(D_{Mesh}+1).$$

Note that since the hardware components used in both topologies are almost equal, we have used one constant for both equations. Considering $C = \varepsilon.E^C_{BS,\ Low}$ we have

$$E_{P,\,WK,\,High} = D_{WK}(1+\alpha+\varepsilon\,T_{WK}) + \varepsilon\,.\,T_{WK}+1$$
$$E_{P,\,Mesh,\,High} = D_{Mesh}(1+\alpha+\varepsilon\,T_{Mesh}) + \varepsilon\,.\,T_{Mesh}+1 \quad (5)$$

Thus the energy consumption ratio in this case equals

$$K = \frac{E_{p,wk,high}}{E_{p,mesh,high}} \text{ or}$$

$$K = \frac{D_{wk}(1+\alpha+\varepsilon\times T_{wk})+\varepsilon\times T_{wk}+1}{D_{mesh}(1+\alpha+\varepsilon\times T_{mesh})+\varepsilon\times T_{mesh}+1} \quad (6)$$

Again, for the sake of present discussion, let us consider specific cases of 16-node mesh and WK-recursive networks.

To calculate the value of T_{wk} and T_{mesh}, we use the average message latencies shown in Fig. 4. It is clear that T_{WK} and T_{Mesh} can be calculated by reducing the average message latency in low traffic load from that in high traffic load. Thus, from Fig. 4(b), we have T_{WK}=63 and T_{mesh}=57, we can write

$$K = \frac{202\varepsilon + 2.21\alpha + 3.21}{209\varepsilon + 2.67\alpha + 3.67}.$$

Fig. 6 shows the K as a function of α and ε. As can be seen in the figure, the values for the case of $\varepsilon = 0$ is the same as Fig. 5 in low traffic region and as the value of ε increases (blocking power increases), power dissipation in the two networks tend to be equal. For smaller values of α, this trend happens quicker.

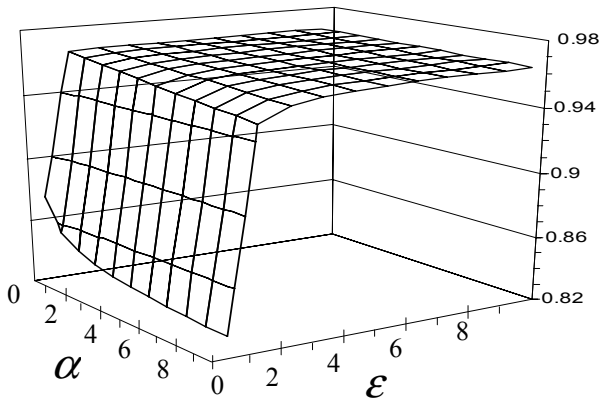


Fig. 6. The ratio of packet transfer power dissipation in the mesh(4x4) and WK(4,2) for different values of α and ε in high traffic region.

V. Conclusion and Future Works

Mesh topology has been used in a variety of interconnection network applications especially for NoC design. However, the WK-recursive network has not been studied yet as the underlying topology for NoCs. In this paper, we proposed a latency and power consumption comparative analysis for these two topologies (mesh and WK-recursive) and showed that the latency of the WK-recursive network for low traffic loads is superior to the mesh topology. The power consumption in the WK-recursive is also less than that of the mesh network for low traffic loads while the power consumption in the two networks is almost equal for high traffic loads. We also proposed a high level approach for modeling the power consumption of the two topologies based on the latency parameters. This approach can be applied to other topologies for NoC designs.

Our next objective is to develop a combined accurate analytical model of power consumption and performance of NoCs and validating it for different network topologies under different working conditions.

References

[1] R. V. Boppana and S. Chalasani, "A framework for designing deadlock-free wormhole routing algorithms", *IEEE Transactions on Parallel and Distributed Systems (TPDS)*, 7(2): 169-183, 1996.

[2] D. R. Duh and G. H. Chen, "Topological properties of WK-recursive networks," *Journal of Parallel and Distributed Computing (JPDC),* 23(3): 468-474, 1994.

[3] C. J. Glass and L. M. Ni, "The turn model for adaptive routing," *Proceedings of the International Symposium on Computer Architecture (ISCA)*, pp. 278-287, 1992.

[4] Y. Hu, H. Chen, Y. Zhu, A. A. Chien and C. Cheng, "Physical synthesis of energy-efficient networks-on-chip through topology exploration and wire style optimizations," *Proceedings of the International Conference on Computer Design (ICCD)*, pp. 111-118, 2005.

[5] D. L. Liu and C. Svensson, "Power consumption estimation in CMOS VLSI chips", *IEEE Journal of Solid-State Circuits (JSSC)*, 29(6): 663-670, 1994.

[6] M. Naderi, B. Javadi, H. Pedram, A. Afzali-Kusha, and M. K. Akbari, "An asynchronous viterbi-decoder for low-power applications", P*roceedings of the Power and Timing Modeling, Optimization and Simulation* (*PATMOS*), pp. 471-480, 2003.

[7] G. D. Vecchia and C. Sanges, "A recursively scalable network VLSI implementation," *Future Generation Computer Systems,* 4(3) 235-243, 1988.

[8] T. T. Ye,"On-chip multiprocessor communication network design and analysis," *Ph.D. dissertation, Stanford University*, 2003.