Large-Scale Atomistic Approach to Random-Dopant-Induced Characteristic Variability in Nanoscale CMOS Digital and High-Frequency Integrated Circuits

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Abstract- **Modeling of device variability is crucial for the accuracy of timing in circuits and systems, and the stability of high-frequency application. Unfortunately, due to the randomness of dopant position in device, the fluctuation of device gate capacitance is nonlinear and hard to be modeled in current compact models. Therefore, a large-scale statistically sound "atomistic" device/circuit coupled simulation approach is proposed to characterize the random-dopant-induced characteristic fluctuations in 16-nm-gate CMOS integrated circuits concurrently capturing the discrete-dopant-number- and discrete-dopant-position-induced fluctuations. The variations of transition time of digital circuit (inverter, NAND, and NOR gates) and high-frequency characteristic of common-source amplifier are estimated. For the digital circuits, the function-dependent and circuit-topology-dependent characteristic fluctuations resulted from random nature of discrete dopants is for the first time discussed. This study provides an insight into random-dopant- induced intrinsic timing and high-frequency characteristic fluctuations. The accuracy of the simulation technique is confirmed by the use of experimentally calibrated transistor physical model.**

Keywords: Device variability, random dopant, fluctuation, timing, digital circuit, high frequency circuit

I. INTRODUCTION

Silicon-based devices are scaled down continually in order to increase density and speed. The gate lengths of scaled metal-oxide-semiconductor field effect transistors (MOSFETs) have been the sub-30 nm for 45 nm node high-performance circuit design [1]. The devices with sub-10-nm-gate lengths have been currently investigated [2,3]. For state-of-art nanometer scale (nanoscale) circuit and system, the local device variation and uncertainty of signal propagation time are crucial for the study of system timing variability [4,5]. Also, the signal propagation time determines the speed of clock. As for the high-frequency circuit and system using state-of-art nanoscale transistors, a cutoff frequency higher than 200 GHz have been experimentally measured [6]. Yield analysis and optimization, which take into account the manufacturing tolerances, model uncertainties, variations in the process parameters, etc., are known as indispensable components of the circuit design methodology [7].

Unfortunately, the attention is seldom drawn to the existence of timing and high-frequency characteristic fluctuations of active device due to random dopant placement. With device scaling, various randomness effects resulting from the random nature of manufacturing process, such as ion implantation, diffusion, and thermal annealing, have induced significant fluctuations of electrical characteristics in nanoscale MOSFETs. The number of dopants is of the order of tens in the depletion region of a nanoscale MOSFET, whose influence on device characteristic is large enough to be distinct [8]. Various random dopant effects have been recently studied in both experimental and theoretical approaches [8-26]. Fluctuations of characteristics are caused not only by a variation in an average doping density, which is associated with a fluctuation in the number of impurities, but also with a particular random distribution of impurities in the channel region. Diverse approaches have recently been reported to study fluctuation-related issues in semiconductor devices [9-21] and circuit [22-26]. However, due to the randomness of dopant position in device, the fluctuation of device gate capacitance is nonlinear and hard to be modeled in current compact models [26]. The effect of the discrete dopants induced timing and high-frequency characteristic fluctuations on nanoscale MOSFET circuit have not been well investigated yet.

In this paper, a statistically sound "atomistic" device/circuit mixed-mode simulation approach is thus employed to analyze the discrete-dopant-induced high-frequency characteristic fluctuations in nanoscale MOSFET circuit, concurrently capturing "dopant

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concentration variation" and "dopant position fluctuation". The statistically generated large-scale doping profiles are similar to the physical process of ion implantation and thermal annealing. Based on the statistically (totally randomly) generated large-scale doping profiles, device simulation is performed by solving a set of three-dimensional (3D) drift-diffusion equations with quantum corrections by the density gradient method [27,28], which is conducted using a parallel computing system [29,30]. In estimation of the timing and high-frequency characteristic fluctuation, to capture the nonlinearity of gate capacitance fluctuation and pursuing higher accuracy [31], a device/circuit coupled simulation [32,33] with discrete dopant distribution is conducted to examine the associated high frequency characteristic fluctuations of circuit, which concurrently considers the discrete-dopant-number- and discrete-dopant-position-induced fluctuations. The accuracy of developed analyzing technique has been quantitatively verified in the experimentally measured characteristics of sub-20 nm devices [10-15].

The paper is organized as follows. In Sec. 2, we introduce the proposed large-scale statistically sound "atomistic" simulation approach for studying the random dopants effect in nanoscale device and circuit. In Sec. 3, we examine the discrete-dopant-induced device-level and circuit-level fluctuations for the 16 nm MOSFET circuit. The fluctuations of transition time and high-frequency characteristics are discussed. Finally, we draw conclusions and suggest future works.

II. The Statistical-Sound Approach for Large-Scale Atomistic Device and Circuit Simulation

The nominal channel doping concentration of the srdued devices is $1.48\text{x}10^{18}$ cm^{-3}. They have a 16 nm gate, a gate oxide thickness of 1.2 nm. In bulk MOSFETs, the characteristic fluctuation is dominated by channel dopants, and the additional effect resulted from source and drain dopants is usually small [21]. Therefore, we only treat the channel dopants discretely.

Figure 1 illustrates the developed simulation flow of the proposed approach. To consider the effect of random fluctuation of the number and location of discrete channel dopants in channel region, 758 dopants are firstly randomly generated in a 80 nm^3 cube, in which the equivalent doping concentration is $1.48\text{x}10^{18}$ cm^{-3} (corresponding to the nominal channel doping concentration), as shown in Fig. 1(a). The 80 nm^3 is then partitioned into sub-cubes of 16 nm^3. The number of dopants may vary from zero to 14, and the average number is six, as shown in Figs. 1(b), 1(c) and 1(d). These sub-cubes are then equivalently mapped into the channel region of the device for the 3D device simulation with discrete dopants, as shown in Fig. 1(e).

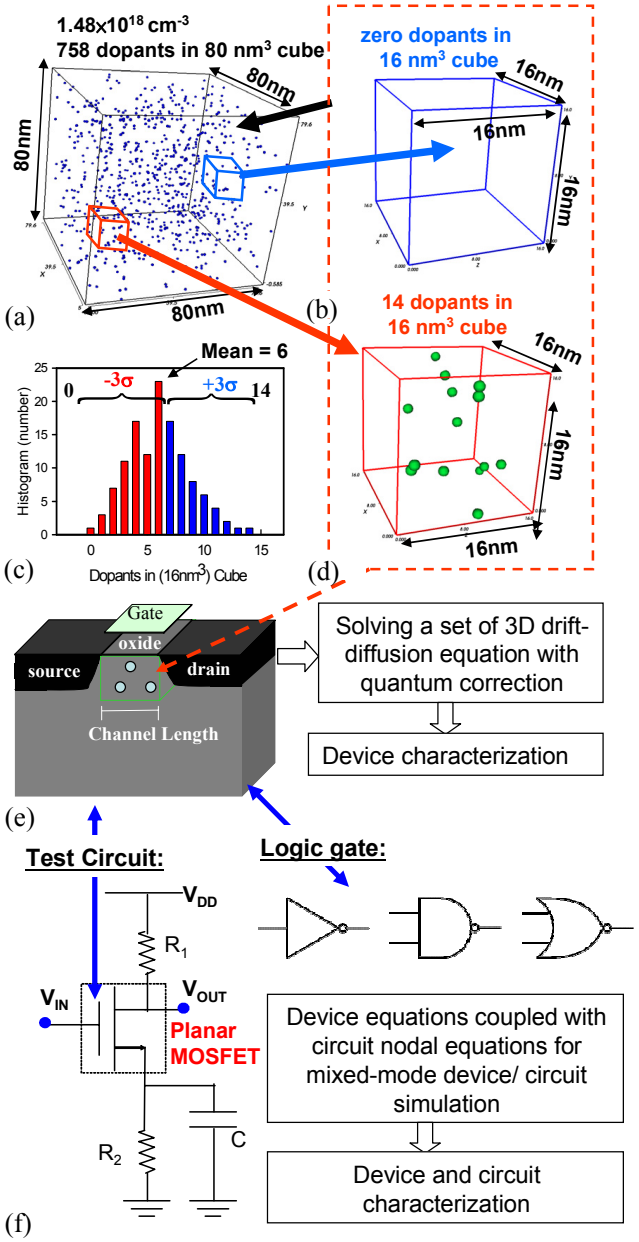

Fig. 1. (a) Discrete dopants randomly distributed in the 80 nm^3 cube with the average concentration of $1.48\text{x}10^{18}$ cm^{-3}. There will be 758 dopants within the cube, but dopants may vary from zero to 14 (the average number is six) within its sub-cubes of 16 nm^3, [(b), (c), and (d)]. The sub-cubes are equivalently mapped into channel region for discrete dopant simulation as shown in (e). To study the random-dopant-induced high-frequency and timing fluctuations in (f) common-source amplifier and logic gates, a 3D atomistic device/circuit coupled simulation is performed.

The device simulation is performed by solving a set of 3D density-gradient equation coupling with drift-diffusion equations [27,28], which is conducted using a parallel computing system [29,30].

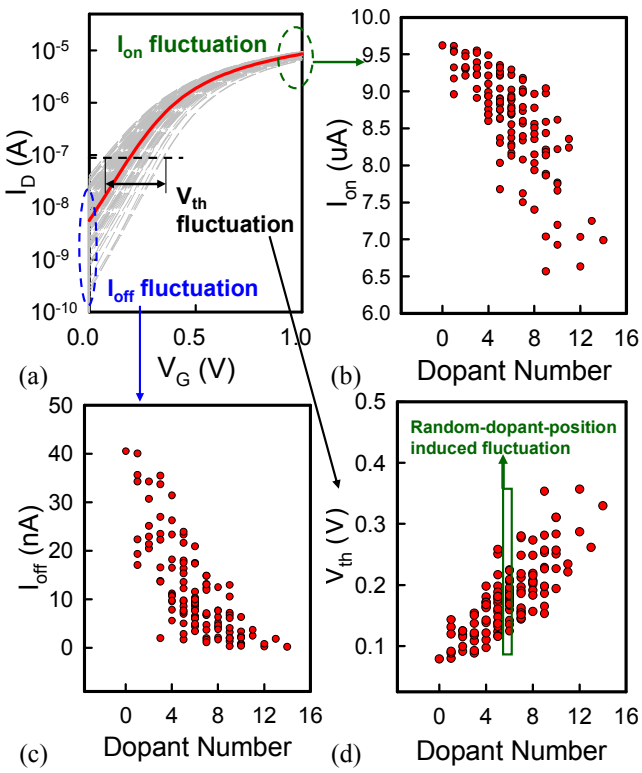

Fig. 2. DC characteristic fluctuations of (a) I_D-V_G characteristics, (b) I_{on}, (c) I_{off}, (d) and V_{th} of the discrete dopant fluctuated 16-nm-gate planar MOSFET. The solid line in I_D-V_G curves shows the capacitance of the nominal case and the dashed lines are random-dopant-fluctuated devices.

Figure 1(f) shows the studied common-source amplifier and the logic gates (inverter, NAND, and NOR) for high-frequency characteristic fluctuations and timing variation estimation, respectively. To investigate the random discrete dopant induced circuit-level fluctuations, and due to the lack of reasonable compact model for describing device gate capacitance, a "atomistic" 3D quantum mechanical simulation of the device coupling with circuit equations are solved [9-13,32,33]. The formulated circuit nodal equations of the tested circuits are directly coupled with aforementioned device equations and then simultaneously solved for device/circuit mixed-mode time-domain and frequency-domain simulation. The input offset voltage of the common-source amplifier is 0.5 V, and the frequency is sweep from $1\text{x}10^8$ Hz to $1\text{x}10^{12}$ Hz. We noted that the proposed simulation technique is statistical sound and computationally cost-effective for random dopant fluctuation characterization. The device mobility and characteristic fluctuation has been validated with the experimentally measured DC base band data [10-15] to ensure the best accuracy.

III. Results and Discussion

In this section the device characteristic fluctuations are investigated. The fluctuations of gate capacitance, cutoff frequency, and intrinsic gate delay of transistor are discussed. The circuit characteristics fluctuations in time-domain and frequency-domain are discussed through the viewpoint of device variability.

A. The Intrinsic Fluctuation of DC Characteristics in Nano-scale MOSFET

Figure 2(a) shows the I_D-V_G characteristics fluctuations of the discrete-dopant-fluctuated 16 nm planar MOSFETs, where the solid line shows the capacitance of the nominal case (continuously doped channel with $1.48\text{x}10^{18}$ cm^{-3} doping concentration) and the dashed lines are random-dopant-fluctuated devices. Each line and symbol in Figs. 2(a)-2(d) indicates its DC characteristic for each device. From the random-dopant-number point of view, the equivalent channel doping concentration is increased when the dopant number increases, which substantially alters the I_D-V_G characteristics, on-state currents (I_{on}), off-state currents (I_{off}), and threshold voltage (V_{th}), shown in Figs. 2(b)-(d), respectively. The threshold voltage is determined from a current criterion that the drain current larger than 10^{-7} (W/L) ampere. As the number of dopants in channel is increased, the device's V_{th} is increased and thus decreases the on-/off-state current. As shown in inset of Fig. 2(d), the position of random dopants induced different fluctuation of characteristics in spite of the same number of dopants. Furthermore, the magnitude of the spread characteristics increases as the number of dopants increases. The detailed physical mechanism is described somewhere else [10-15].

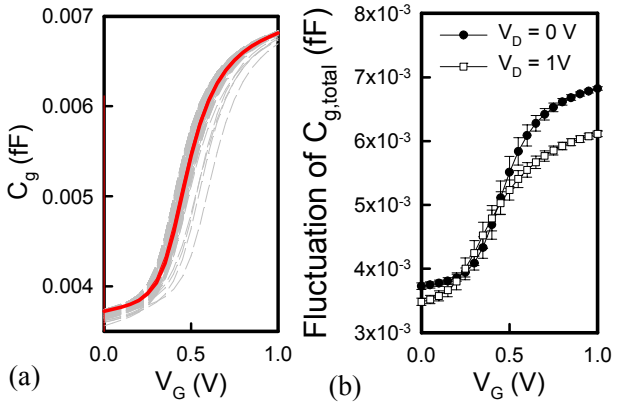

Fig. 3. (a) Capacitance-voltage characteristics (b) and fluctuations of gate capacitance with different drain biases for the discrete-dopant-fluctuated 16-nm-gate planar MOSFET, where the solid line shows the capacitance of the nominal case and the dashed lines are random-dopant-fluctuated devices.

B. *The Gate-Capacitance and Related Characteristic Fluctuations of in Nano-scale MOSFET*

The capacitance-voltage characteristics of the discrete-dopant-fluctuated 16 nm planar MOSFETs are investigated in Fig. 3(a), where the solid line shows the capacitance of the nominal case and the dashed lines are the random-dopant-fluctuated devices. The lateral shift and change of shape for the capacitance-voltage characteristics are observed. The variation of gate capacitance is resulted from the random dopant placement in channel depletion region. The lateral shift of gate capacitance is resulted from the variation of V_{th}, and may be described by the correspond parameters in compact model. However, for the variation of shape of capacitance-voltage curves, the variation is determined by the position of random dopants in channel, which is hard to be described in current compact model [26]. To the best of our knowledge, the variation of gate capacitance has not been modeled yet. The fluctuation of the gate capacitance (C_g) with different drain bias is studied in Fig. 3(b). Result shows that the device operates under saturation operation may suffer form the less gate capacitance fluctuation, where the screening effect of inversion layer of device screens the variation of electrostatic potential and decreases the fluctuation of gate capacitance [26].

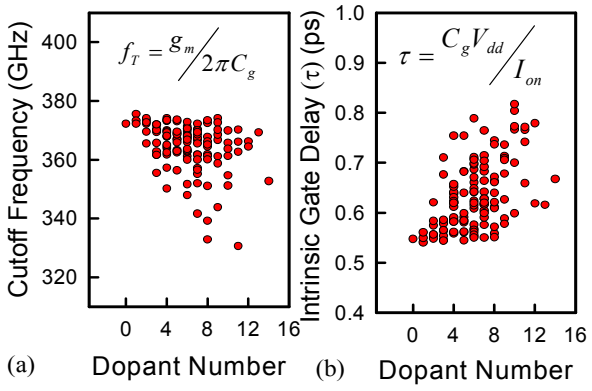

Fig. 4. (a) Cutoff frequency (b) and intrinsic gate delay of transistor for the discrete-dopant-fluctuated 16-nm-gate planar MOSFETs.

The intrinsic cutoff frequency and intrinsic gate delay of the studied device are studied in Figs. 4(a) and 4(b), respectively, in which the insets give the definition of these characteristics. As the number of dopant in device channel is increased, the depletion width is decreased, and then increases the gate capacitance. With the decreasing transconductance and increasing gate capacitance, the intrinsic cutoff frequency of the studied device is decreased as the dopant number is increased. As for the intrinsic gate delay of the studied device, with decreasing on-state current and increasing gate capacitance, the intrinsic gate delay is increased as the dopant number is increased. The fluctuations of cutoff frequency and intrinsic gate delay are 8.2 GHz and 0.069 ps, respectively, and the magnitude of fluctuation is increased as dopant number is increased.

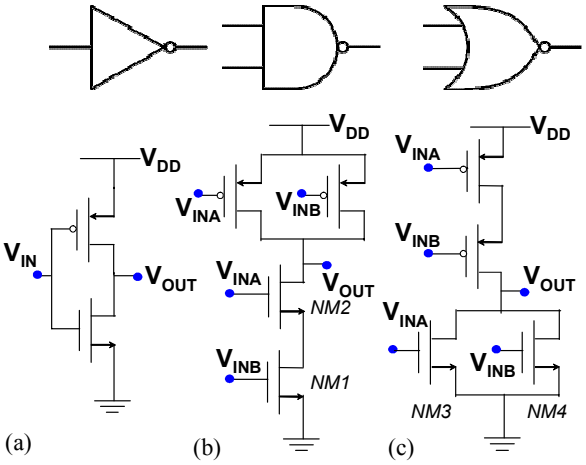

Fig. 5. The studied 16-nm-gate (a) inverter, (b) NAND, (c) and NOR logic circuits.

C. *The Device Variability Induced Fluctuations in Logic Circuits*

The transition characteristics of the logic gate, the inverter, two-input NAND, and two-input-NOR gates are implemented and studied as shown in Figs. 5(a)-5(c), respectively. The input and output signal for the studied logic circuits are shown in Figs. 6(a)-6(c), in which the solid line shows the capacitance of the nominal case (continuously doped channel with 1.48×10^{18} cm^{-3} doping concentration) and the dashed lines are random-dopant-fluctuated devices. The rise time and fall time for the discrete-dopant-fluctuated circuits are calculated and summarized in Table I, where the rise time is defined as the time required for the output voltage to go from 10% of the logic "1" level to 90% of the logic "1", and the fall time is defined as the time required for the output voltage to go from 90% of the logic "1" level to 10% of the logic "1" level. The delay time is the difference in times between 50% points of input and output signal. For all of the studied circuits, the rise time fluctuation is larger than the fall time fluctuation because of the smaller driving current of p-type MOSFET than that of n-type one. The device with larger transconductance may require less time to charge and discharge the given gate capacitance and thus show a less timing fluctuations.

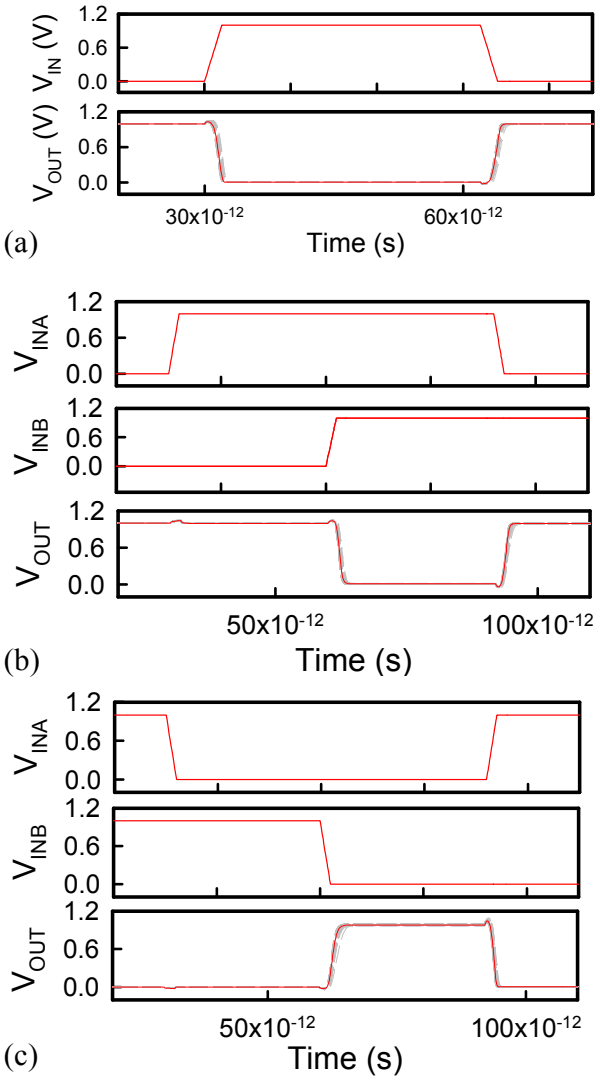

Fig. 6. The input and output signal for the studied discrete-dopant-fluctuated 16-nm-gate (a) inverter, (b) NAND, (c) and NOR circuits.

Also, we can expect that a logic circuit with fewer transistors, such as an inverter circuit, may have a less variation of characteristics due to the less of fluctuation sources. Nevertheless, the variation of timing characteristics may suffer from the increase of transistors in circuit. It's thus reasonable to infer that the NAND and NOR circuits may exhibit larger timing fluctuations than the inverter circuit. Also, they may have similar timing fluctuations due to the same number of transistor in circuit. However, the obtained results show that the rise time and fall time fluctuations for the NAND gate are 0.53 and 1.87 times larger than that of the NOR gate. The characteristic difference of timing fluctuation is resulted from the different device's characteristic fluctuations with different input signal. For the fall time transition characteristics in the NAND and NOR gates, their output signal transitions are determined by the devices NM1 and NM3 in Figs. 5(b) and 5(b), respectively, where the NM1 MOSFET is operated in linear region, and the NM3 MOSFET is operated in saturation region. As studied in Fig. 3(b), the device operated in saturation region may exhibit a less gate capacitance fluctuation. Moreover, the n-type MOSFET transistors in series for the NAND gate may introduce addition variations to influence the operation of NM1. Therefore, the fall time fluctuation of the NAND gate is larger than that of the NOR gate due to the different device's operation characteristics and circuit topology. In other words, the fluctuation of timing characteristics may be influenced by the different input signal in circuit. Similarly, we can infer that the rise time transition of the NOR gate is larger than that of the NAND gate.

TABLE I
SUMMARIZED TRANSITION TIME VARIATION FOR THE 16-NM-GATE LOGIC GATE CIRCUITS. (* NORMALIZED BY THE NOMINAL VALUE)

Nominal Rise Time (unit: ps)	Nominal Fall Time	Nominal Delay Time (low-to-high)	Nominal Delay Time (high-to-low)
INVERTER			
1.021	0.897	0.800	0.590
NAND			
1.248	1.197	0.987	1.254
NOR			
1.762	0.993	1.616	0.761
Rise Time Fluctuation	Fall Time Fluctuation	Delay Time Fluctuation (low-to-high)	Delay Time Fluctuation (high-to-low)
INVERTER			
0.036	0.021	0.105	0.108
NAND			
0.070	0.056	0.107	0.129
NOR			
0.133	0.030	0.169	0.111

For the delay time fluctuation, similarly, the circuit with few transistors may exhibit less variation of characteristics due to the less fluctuation sources. Thus, the delay time fluctuation of the inverter gate is smaller than that of NAND and NOR gates. Besides the signal transition time fluctuation, the delay time fluctuation will also include the fluctuation of the transition point resulted from threshold voltage fluctuation. Therefore, the delay time fluctuation is significantly larger than the rise/fall time fluctuations. Moreover, due to the less threshold voltage fluctuation of p-type MOSFETs, the low-to-high delay time fluctuation is smaller than the high-to-low delay time fluctuation. The function- and circuit-topology-dependent characteristic fluctuations resulted from random nature of discrete dopants is for the first time briefly discussed and worth to be explored

for future digital circuit applications in nano-CMOS era.

D. The DC Transfer and High-Frequency Characteristic Fluctuations in Nano-scale MOSFET Circuits

In this subsection, the DC transfer and high-frequency characteristic fluctuations of the common-source amplifier, as displayed in Fig. 1(f), are discussed.

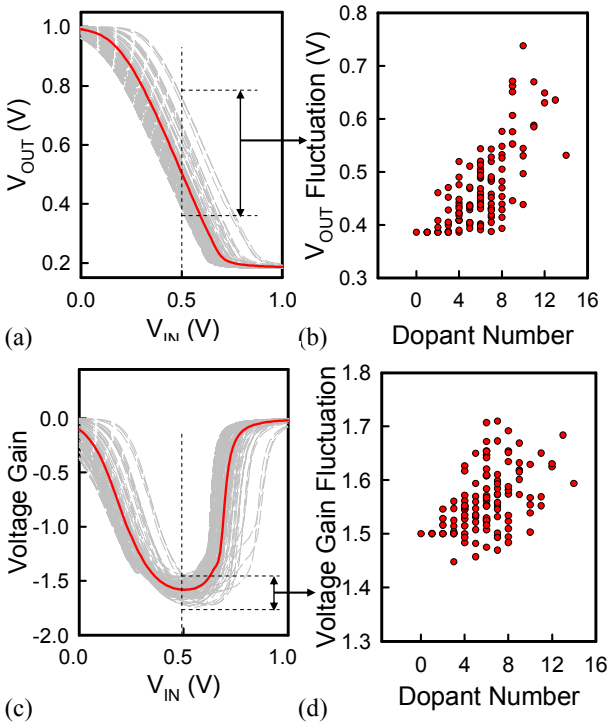

Fig. 7. The (a) voltage-transfer-curve (VTC), (b) the output voltage (V_{out}), (c) the voltage gain, (d) and the fluctuation of voltage gain for the studied discrete-dopant-fluctuated 16-nm-gate common-source circuits. The solid line shows the capacitance of the nominal case (continuously doped channel with $1.48x10^{18}$ cm^{-3} doping concentration) and the dashed lines are the random-dopant-fluctuated devices.

Figure 7 explores the DC characteristic fluctuation of the studied circuit. The voltage-transfer-curve (VTC) and corresponding output voltage (V_{out}) of the discrete-dopant-fluctuated 16nm-gate planar MOSFET circuits are studied in Figs. 7(a) and 7(b), where the input offset voltage is 0.5 V. The derived voltage gain and its fluctuation of the studied circuit are shown in Figs. 7(c) and 7(d). The V_{out} is increased as the number of dopant in device channel is increased due to the decreasing output current and voltage drop across R_1. The variation of V_{out} will influence the capacitance of the studied MOSFETs and alters the high frequency response. Moreover, as expected, the fluctuations of V_{out} and voltage gain are increased as dopant number is increased.

Figure 8(a) explores the high-frequency circuit gain as a function of operation frequency for all fluctuated cases, where the solid line shows the nominal case, whose channel doping profile is continuously doped with $1.48x10^{18}$ cm^{-3}. The circuit gain, 3dB bandwidth, and unity-gain bandwidth of the nominal case are 8.14 dB, 68 GHz, and 281 GHz, respectively. The corresponding high-frequency characteristic fluctuations for the studied circuit are shown in Figs. 8(b)-8(d), where the three expressions within each plot show the trend of circuit gain, 3dB bandwidth, and unity-gain bandwidth as a function of device characteristic and circuit element.

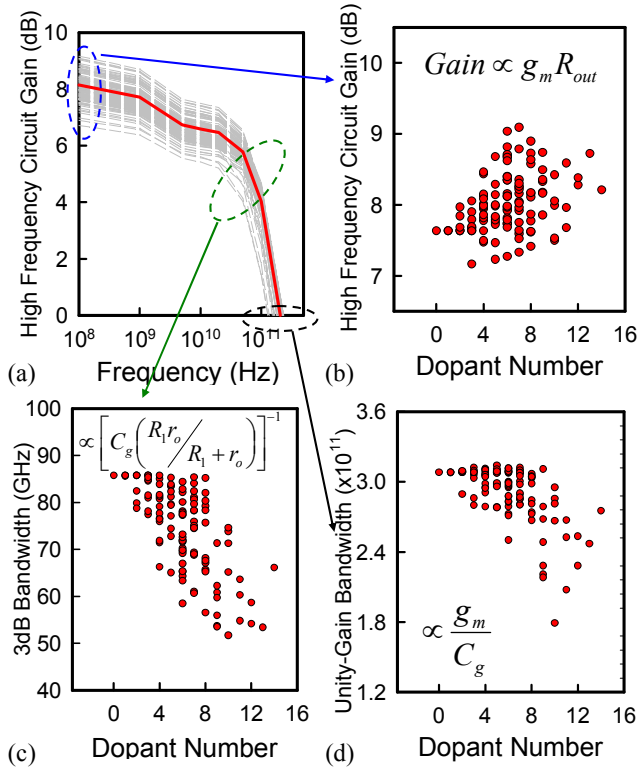

Fig. 8. The (a) frequency response, (b) high-frequency circuit gain, (c) 3dB bandwidth, (d) and unity-gain bandwidth fluctuations of the studied discrete-dopant-fluctuated 16-nm-gate common-source circuits.

The gain of the studied circuit is proportional to transconductance (g_m) multiplied by output resistance of circuit. The circuit output resistance, R_{out}, is given by inverse of ($I_{OUT}/V_{OUT} + r_o^{-1}$), where I_{out} and V_{out} are the output current and voltage of the studied circuit; r_o is the intrinsic resistance of transistor. The dependence of r_o in device on threshold voltage is given below:

$$r_o = \frac{\partial V_{ds}}{\partial I_D} \propto \frac{1}{(V_{GS} - V_{th})^2}. \quad (1)$$

Although the dependence of R_{out} and g_m on threshold voltage is inverse, the trend of circuit gain fluctuation is dominated the output resistance due to the square dependence of r_o on V_{GS}-V_{th}. Therefore, the trend of circuit gain fluctuation is dominated by the output resistance and increased as number of dopant is increased, as shown in Fig. 8(b). Moreover, the trend of the high frequency circuit gain is similar to the voltage gain, as shown in Fig. 7(d).

As for the 3dB bandwidth and the unity-gain bandwidth in Figs. 8(c) and 8(d). When the number of dopant in device channel is increased, the depletion width is decreased, and it thus increases the gate capacitance. The fluctuation of C_g accompanied with increasing r_o and decreasing g_m result in a decrement of 3dB bandwidth and the unity-gain bandwidth on increasing dopant number. Similar to the DC characteristic of device, the high-frequency characteristic fluctuation of the nanoscale MOSFET circuit is much more scattered as number of dopants is increased. The standard deviations of the gain, 3dB bandwidth, unity-gain bandwidth, and gain-bandwidth product are summarized in Table II. For the studied 16-nm-gate MOSFET circuit, the number of discrete dopants, varying from zero to 14, may result in 5.7% variation of the circuit gain, 14.1% variation of the 3dB bandwidth, and 10.4% variation of the unity-gain bandwidth.

TABLE II
UNITS FOR MAGNETIC PROPERTIES SUMMARIZED HIGH-FREQUENCY CHARACTERISTIC FLUCTUATIONS OF THE NANO-MOSFET CIRCUIT.

	Gain (dB)	3dB bandwidth (Hz)	Unity-gain bandwidth (Hz)
Nominal	8.138	6.84×10^{10}	2.81×10^{11}
Standard deviation	0.465	9.63×10^{9}	2.93×10^{10}
Variation	0.057	0.141	0.104

IV. CONCLUSIONS

In this paper, a 3D "atomistic" device/circuit simulation technique has been proposed to investigate the random-dopant-induced characteristic fluctuations in nanoscale CMOS digital (inverter, NAND, and NOR gates) and high-frequency integrated circuits, concurrently capturing the random discrete-dopant-number- and random discrete-dopant-position-induced fluctuations. To capture the nonlinearity of device gate capacitance fluctuation and to provide accurate estimation of transition time and high-frequency characteristic of nanoscale CMOS circuits, the device/circuit coupled mixed-mode simulation is performed. For the digital circuits, the function-dependent and circuit-topology-dependent characteristic fluctuations resulted from random nature of discrete dopants is for the first time discussed. Using the experimentally calibrated analyzing technique, the result have shown that the discrete-dopant fluctuated 16 nm MOSFET circuit exhibits 5.7% variation of the circuit gain, 14.1% variation of the 3dB bandwidth and 10.4% variation of the unity-gain bandwidth. This study provides an insight into random-dopant- induced intrinsic timing and high-frequency characteristic fluctuations. The experimental and theoretical verification will benefit the development of state-of-art digital and high-frequency circuits design with accurate timing and stable performance. We are now studying the fluctuation suppression technique for nanoscale MOSFET circuit and system.

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REFERENCES

[1] D. M. Fried, J. M. Hergenrother, A. W. Topol, L. Chang, L. Sekaric, J. W. Sleight, S. McNab, J. Newbury, S. Steen, G. Gibson, Y. Zhang, N. Fuller, J. Bucchignano, C. Lavoie, C. Cabral, D. Canaperi, O. Dokumaci, D. Frank, E. Duch, I. Babich, K. Wong, J. Ott, C. Adams, T. Dalton, R. Nunes, D. Medeiros, R. Viswanathan, M. Ketchen, M. Ieong, W. Haensch, and K. W. Guarini, "Aggressively scaled (0.143 μm2) 6T-SRAM cell for the 32 nm node and beyond," in *Int. Electron Devices Meeting Tech. Dig.*, pp. 261-264, Dec. 2004.

[2] H. Lee, L.-E. Yu, S.-W. Ryu, J.-W. Han, K. Jeon, D.-Y. Jang, K.-H. Kim, J. Lee, J.-H. Kim, S. C. Jeon, G. S. Lee, J. S. Oh, Y. C. Park, W. H Bae, H. M. Lee, J. M. Yang, J. J. Yoo, S. I. Kim and Y.-K. Choi, "Sub-5nm All-Around Gate FinFET for Ultimate Scaling," in *VLSI Technol. Tech. Symp. Dig.*, pp. 58-59, 2006.

[3] F.-L. Yang, D.-H. Lee, H.-Y. Chen, C.-Y. Chang, S.-D. Liu, C.-C. Huang, T.-X. Chung, H.-W. Chen, C.-C. Huang, Y.-H. Liu, C.-C. Wu, C.-C. Chen, S.-C. Chen, Y.-T. Chen, Y.-H. Chen, C.-J. Chen, B.-W. Chan, P.-F. Hsu, J.-H. Shieh, H.-J. Tao, Y.-C. Yeo, Y. Li, J.-W. Lee, P. Chen, M.-S. Liang, and C. Hu, "5nm-gate nanowire FinFET," in *VLSI Technol. Tech. Symp. Dig.*, pp. 196-197, June 2004.

[4] K. Shinkai, M. Hashimoto, A Kurokawa, and T. Onoye, "A Gate Delay Model Focusing on Current Fluctuation over Wide-Range of Process," in *Proc. Of Int. Conf. on Computer-Aided Design (ICCAD)*, 2006, pp. 47-52.

[5] B. Cline, K. Chopra, D. Blaauw, and Cao Yu, "Analysis and Modeling of CD Variation for Statistical Static Timing," in *Proc. Of Int. Conf. on Computer-Aided Design* (*ICCAD*), 2006, pp. 60-66.

[6] V. Dimitrov, J. B. Heng, K. Timp, O. Dimauro, R. Chan, J. Feng, W. Hafez, T. Sorsch, W. Mansfield, J. Miner, A. Kornblit, F. Klemens, J. Bower, R. Cirelli, E. Ferry, A. Taylor, M. Feng, and G. Timp, "High Performance, sub-50nm MOSFETS for Mixed Signal Applications," in *Int. Electron Devices Meeting Tech. Dig.*, pp. 213-216, Dec. 2005.

[7] Q. Li, J. Zhang, Wei Li, J. S. Yuan, Yuan Chen, and Anthony S. Oates, "RF Circuit Performance Degradation Due to Soft Breakdown and Hot-Carrier Effect in Deep-Submicrometer CMOS Technology," *IEEE Trans. Microwave Theory Tech.*, vol. 49, no. 9, pp. 1546-1551, Sept. 2001.

[8] H.-S. Wong, Y. Taur, and D. J. Frank, "Discrete Random Dopant Distribution Effects in Nanometer-Scale MOSFETs," *Microelectronics Reliability*, vol. 38, no. 9, pp. 1447-1456, Sept. 1999.

[9] Y. Li and S.-M. Yu, "Comparison of Random-Dopant-Induced Threshold Voltage Fluctuation in Nanoscale Single-, Double-, and Surrounding-Gate Field-Effect Transistors," *Jpn. J. Appl. Phys.*, vol. 45, no. 9A, pp. 6860-6865, Sept. 2006.

[10] F.-L. Yang, J.-R. Hwang, H.-M. Chen, J.-J. Shen, S.-M. Yu, Y. Li, and Denny D. Tang, "Discrete Dopant Fluctuated 20nm/15nm-Gate Planar CMOS," in *VLSI Technol. Tech. Symp. Dig.*, pp. 208-209, June 2007.

[11] F.-L. Yang, J.-R. Hwang, and Y. Li, "Electrical Characteristic Fluctuations in Sub-45nm CMOS Devices," in *IEEE Custom Integrated Circuits Conf.*, pp. 691-694, Sept. 2006.

[12] Y. Li, and C.-H Hwang, "Electrical characteristic fluctuations in 16nm bulk-FinFET devices", *Microelectronics Engineering*, vol. 84, no. 9-10, pp.2093-2096, Sept.-Oct. 2007.

[13] Y. Li, and C.-H Hwang, "Discrete-dopant-induced characteristic fluctuations in 16 nm multiple-gate silicon-on-insulator devices", *J. Appl. Phy.*, vol. 102, no. 8, 084509, 2007.

[14] Y. Li, and S.-M. Yu, "A Coupled-Simulation-and-Optimization Approach to Nanodevice Fabrication With Minimization of Electrical Characteristics Fluctuation," *IEEE Trans. Semi. Manufacturing*, vol. 20, no. 4, pp.432-438, Nov. 2007.

[15] Y. Li, and S.-M. Yu, "A study of threshold voltage fluctuations of nanoscale double gate metal-oxide-semiconductor field effect transistors using quantum correction simulation," *J. Comp. Elect.*, vol. 5, no. 2-3, pp. 125-129, July 2006.

[16] A. Asenov, "Random Dopant Induced Threshold Voltage Lowering and Fluctuations in Sub-0.1 um MOSFET's: A 3-D "Atomistic" Simulation Study," *IEEE Trans. Electron Device*, vol. 45, no. 12, pp. 195-200, Dec. 1998.

[17] A. Asenov and S. Saini, "Suppression of Random Dopant-Induced Threshold Voltage Fluctuations in Sub-0.1-um MOSFET's with Epitaxial and -Doped Channels," *IEEE Trans. Electron Device*, vol. 46, no. 8, pp. 1718-1724, Aug. 1999.

[18] K. Noda, T. Tatsumi, T. Uchida, K. Nakajima, H. Miyamoto, and C. Hu, "A 0.1- m delta doped MOSFET fabricated with post-low-energy implanting selective epitaxy," *IEEE Trans. Electron Device*, vol. 45, no. 4, pp. 809–813, Apr. 1998.

[19] G. Roy, A. R. Brown, F. Adamu-Lema, S. Roy, and A. Asenov, "Simulation Study of Individual and Combined Sources of Intrinsic Parameter Fluctuations in Conventional Nano-MOSFETs," *IEEE Trans. Electron Device*, vol. 53, no. 12, pp. 3063-3070, Dec. 2006.

[20] W. J. Gross, D. Vasileska, and D. K. Ferry," A novel approach for introducing the electron-electron and electron-impurity interactions in particle-based simulations," *IEEE Electron Device Letter*, vol. 20, no. 9, pp. 463-465, Sept. 1999.

[21] D. J. Frank, Y. Taur, and H.-S. P. Wong, "Monte Carlo modeling of threshold variation due to dopant fluctuations," in *Proc. Symp. VLSI Technology*, 1999, pp. 169–170.

[22] R. Tanabe, Y. Ashizawa, H. Oka, "Investigation of SNM with Random Dopant Fluctuations for FD SGSOI and FinFET 6T SOI SRAM Cell by Three-dimensional Device Simulation," in *Simulation of Semiconductor Processes and Device Conf.*, pp. 103-106, Sept. 2006.

[23] B. Cheng, S. Roy, G. Roy, and A.Asenov, "Impact of Intrinsic Parameter Fluctuations on SRAM Cell Design," in *Int. Solid-State and Integrated Circuit Technology Conf.*, pp. 1290-1292, Oct. 2006.

[24] H. Mahmoodi, S. Mukhopadhyay, and K. Roy," Estimation of delay variations due to random-dopant fluctuations in nanoscale CMOS circuits," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 9, pp. 1787-1796, Sept. 2005.

[25] B. Cheng, S. Roy, G. Roy, A. Brown, and A.Asenov, "Impact of Random Dopant Fluctuation on Bulk CMOS 6-T SRAM Scaling," in *Proc.36th European Solid-State Device Research Conf.*, pp. 258-261, Sept. 2006.

[26] A. Brown and A. Asenov, "Capacitance fluctuations in bulk MOSFETs due to random discrete dopants," *J. Comp. Elect.*, Jan. 2008. DOI:10.1007/s10825-008-0181-y.

[27] S. Odanaka, "Multidimensional discretization of the stationary quantum drift-diffusion model for ultrasmall MOSFET structures," *IEEE Trans. Computer-Aided Design Integr. Circuit and Sys.*, vol. 23, no. 6, pp.837-842, June 2004.

[28] G. Roy, A. R. Brown, A. Asenov, and S. Roy, "Quantum Aspects of Resolving Discrete Charges in 'Atomistic' *Device Simulations," J. Comp. Elect.*, vol. 2, no. 2-4, pp. 323-327, Dec. 2003.

[29] Y. Li and S.-M. Yu, "A Parallel Adaptive Finite Volume Method for Nanoscale Double-gate MOSFETs Simulation," *J. Comp. Appl. Math.*, vol. 175, no.1, pp. 87-99, Mar. 2005.

[30] Y. Li, S. M. Sze, and T.S. Chao, "A Practical Implementation of Parallel Dynamic Load Balancing for Adaptive Computing in VLSI Device Simulation," *Eng. with Comp.*, vol. 18, no. 2, pp. 124-137, Aug., 2002.

[31] T. Grasser, and S. Selberherr, "Mixed-mode device simulation," *Microelectronics Journal*, vol. 31, no. 11-12, pp.873-881, Dec. 2000.

[32] K.-Y. Huang, Y. Li, and C.-P. Lee, "A time-domain approach to simulation and characterization of RF HBT two-tone intermodulation distortion," *IEEE Trans. Microwave Theory and Tech.*, vol.51, no.10, pp.2055-2062, Oct. 2003.

[33] Y. Li, J.-Y. Huang and B.-S. Lee, "Effect of single grain boundary position on surrounding-gate polysilicon thin film transistors," *Semiconductor Science and Technology*, vol. 23, 015019, 2008.