Advanced Analog Filters for Telecommunications

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Abstract - **In this paper advances on analog filter design for telecom transceivers are addressed. Portable devices require a strong power consumption reduction to increase the battery life. Since a considerable part of the power consumption is due to the analog baseband filters, improved and/or novel analog filter design approaches have to be developed. In this paper some advances on this field reported in last years are summarized. Each design (developed for different standards) exploits the standard specifications with different architectures and circuit strategies devoted to power consumption reduction. The first is for reconfigurable Bluetooth/UMTS/WLAN receivers, the second is for very-low voltage (550mV) WLAN receivers, the third one is for impulse-radio UWB receivers, while the fourth is for very low-power OFDB-UWB receivers.**

I. INTRODUCTION

Technical evolution and market requirements demand for high-performance fully integrated telecom transceivers. The most popular receiver architecture is the Direct Conversion (DC) one: for this case the following discussion is applied. Fig. I shows the typical DC receiver architecture.
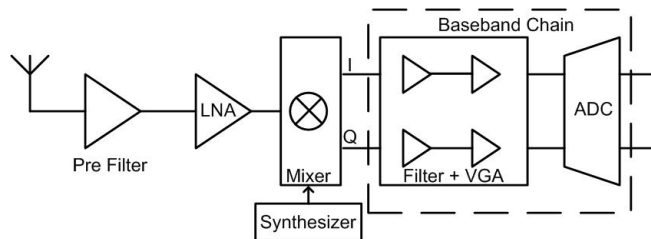

Fig. I – DC receiver architecture

The signal from the antenna is processed by an external prefilter to reject an amount of the out-of-band interferers. The front-end consists of LNA and a quadrature mixer that downconverts the signal. The baseband part is composed by the low-pass filter (LPF), the variable gain amplifier (VGA) and the analog to digital converter (ADC). LPF and VGA perform the following functions:

-   The LPF selects the channel and reduces the noise and the out-of-band interferes, relaxing ADC requirements.

-   The VGA increases the in-band input signal in order to optimize analog to digital conversion performed by the following ADC. For example in the UWB systems the input signal power is typically very low (about -40dBm)

therefore it need to be amplified by more then a 40dB factor.

The LPF can be implemented with different solutions, depending on several reasons as:
- the power consumption minimization is strongly required by portable devices to increase the battery life;
- different communication standards require strongly different analog baseband filters performances in terms of bandwidth, distortion, SNR, SNDR, etc….;
- the use of advanced CMOS technologies is forced by the digital part. Scaled CMOS technologies are critical for analog design for several poorer CMOS device parameters like threshold voltage and output impedance. Scaled CMOS technologies feature a decreasing MOS minimum channel length that operates only at low supply voltage (in the order of 1V-1.2V, or even below). At the supply reduction, a lower threshold voltage (V_{TH}) results, for leakage currents limitation, resulting in a decreasing effective space V_{DD}-V_{TH}. Also output impedance in scaled CMOS technologies is decreasing and this results in lower accuracy and poorer linearity.

Considering the state of the art of the RF Transceivers for telecom systems, a constant increasing of the input signal bandwidth is observed [1],[2],[3]. Considering the power consumption of the entire transceiver increases with the input signal bandwidth, the low power low voltage analog filters are a key issue, due the significant baseband path contribution on the overall receivers power consumption, (about 20%). In the Fig. II the behavior of the input signal bandwidth and of the correspondent power consumption for the zero-IF RF receivers case vs. different standard is shown.

A key problem of a telecom LPF is that strong out-of band interferes are present, so that high-selectivity filters are needed. Furthermore the coexistence of different signals in adjacent bandwidths requires large inter-modulation product rejection, so large linearity performance. For this linearity requirement, the most popular LPF approach in the DC receivers is the Active-RC topology. The Active-RC biquadratic cell features large linearity and strong frequency response accuracy. However, an Active-RC integrator introduces an additional pole at its opamp unity gain bandwidth (UGB). This reduces the frequency response accuracy. For this reason, the opamp UGB has to be ≈100

higher than the filter pole frequency, resulting in large power consumption and challenges to guarantee a sufficiently large dc-gain. On the other hand, the g_m-C biquad appears the most feasible solution in order to save the current consumption and to maintain low input referred noise, but at the cost of lower linearity, which is a critical point in the telecom systems. No optimum solution is present and the design has to be strongly customized case by case. In this paper some innovative solutions are proposed. All of them demonstrate that the specifications of a given system can be exploited to design new conceptual structures able to reduce power consumption. The proposed solutions are examples of different circuit solutions and are developed for different systems. The first is for reconfigurable Bluetooth/UMTS/WLAN receivers where an innovative Active-gm-RC topology has been introduced [4]. The second is for very-low voltage (550mV) WLAN receivers, which demonstrates that challenging linearity performance can be achieved also at very low-voltage[5]. The third one is for impulse-radio UWB receivers, where the reduced linearity requirements are used for a strong power consumption reduction[6]. For each section the experimental results are reported to validate the proposed circuital solution.
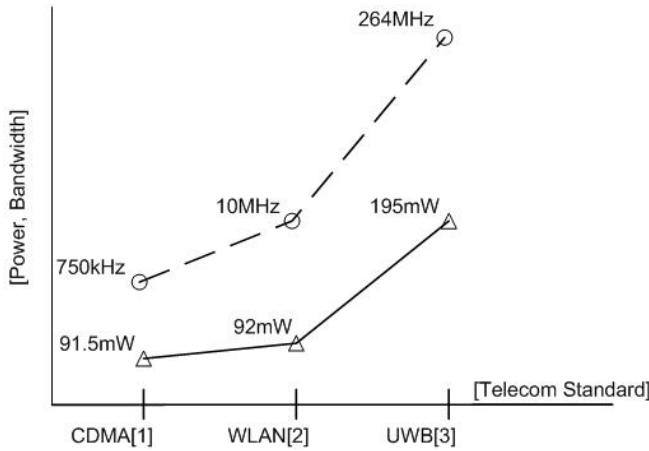

Fig. II - RF Transceivers Bandwidth and Power Trend

II. RECONFIGURABLE ACTIVE-g_m-RC FILTER

A solution to overcome the frequency response inaccuracy, introduced by the 2nd pole of the Active-RC integrator, is represented by the Active-gm-RC structure. In addition, it reduces noise and current consumption while maintaining large in-band linearity. The Active-g_m-RC biquadratic cell is presented in the Fig. III.
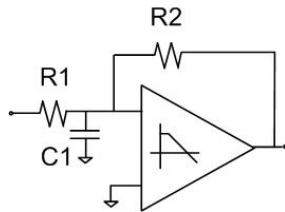

Fig. III – Active Gm-RC Biquadratic Cell

The key concept of this cell is that the opamp frequency response is exploited to synthesize the biquad complex poles pair. In particular the opamp is used as open-loop integrator in a feedback configuration. So that considering the integrator UGBW is comparable with the filter poles frequency, the current consumption of the opamp is strongly reduced with respect than the typical closed-loop topologies. Only two resistors and one capacitance are used to synthesize two complex poles so that lower noise and smaller area is performed with respect the single opamps Active-RC cells. Then large in-band linearity is guaranteed due to the close-loop topology. The cell dc-gain (G), poles frequency (ω_o), and quality factor (Q) are here reported.

$$G = \frac{R2}{R1}, \quad \omega_o = \sqrt{\frac{\omega_u}{C1 \cdot R2}}, \quad Q = \frac{1}{1+G}\sqrt{\omega_u C1 \cdot R2} \quad \textbf{(i)}$$

Fig. IV shows the 4th-order UMTS/WLAN reconfigurable filter. It is the cascade of two Active Gm-RC biquad cells.
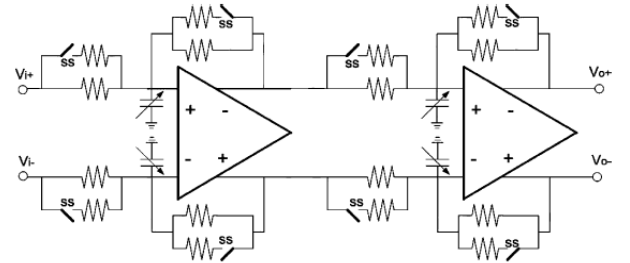

Fig. IV – A programmable 4th–order Active-g_m-RC Filter

The filter features programmable gain and bandwidth in order to operate with different standards. The opamp is optimized in terms of power consumption and noise performance depending on the selected standard. Fig. V shows the opamp schematic.
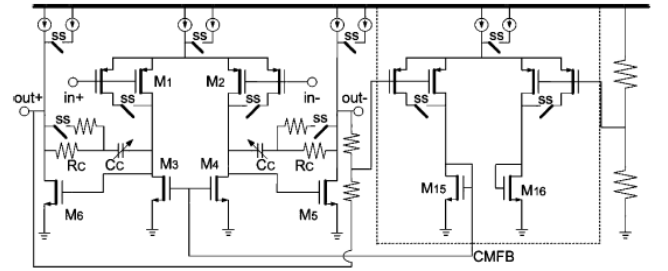

Fig. V – Class-A reconfigurable opamp

The opamp is a class A topology. The current flowing by the input and output stage is adequately set by the control bit SS. Also the opamp differential input pair is set in order to optimize the input stage transconductance with respect the filter specifications. In this way an efficient dual-mode filter in terms of power, area and noise operating at 1.2V supply voltage has been realized. Fig. VI shows the programmable frequency response of the LPF and VGA in the reconfigurable UMTS/WLAN receiver. The LPF is the just presented design and the VGA gives the amount of gain needed for the output signal power requirements. A

performance summary for the Active-g_m-RC filter is reported in the Tab. I. Fig. VII shows the chip photo.
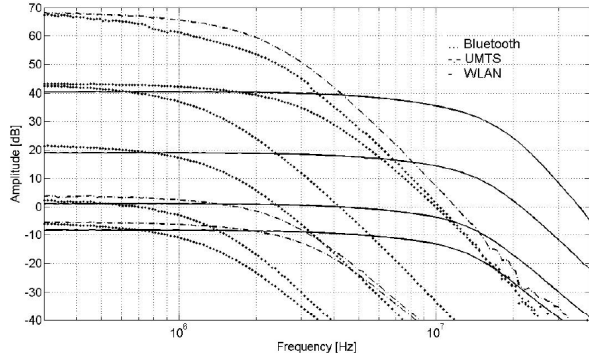

Fig. VI – Active-g_m-RC LPF and VGA Programmable Frequency Response

	UMTS	WLAN
Technology	0.13μm CMOS	
Supply Voltage	1.2V	
Die area occupation	0.9mm2	
Transfer Function	4th order Bessel	
f-3dB	2.11MHz	11MHz
Max f-3dB Deviation	5%	
Filter dc-gain	4dB	
IRN	36μV$_{rms}$	36μV$_{rms}$
In-band IIP3	21dBm	21dBm
DR(THD=-40dBc)	81dB	81dB
Out-of-band IIP3	31dBm	
Power Consumption	3.4mW	14.2mW

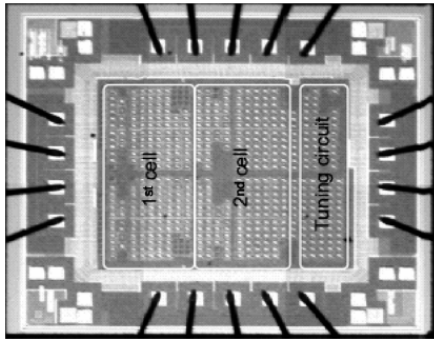Tab. I – Active-g_m-RC Performance Resume

Fig. VII – Active-g_m-RC Filter Chip Photo

III. A 0.55V SUPPLY VOLTAGE ANALOG FILTER

The continuous reduction of the supply voltage is requiring for solution capable of operating at lower supply voltage while guaranteeing large linearity. Efficient solutions to design sub-1V analog filters with switched-capacitors techniques are already available [8], but with reduced bandwidth. On the other hand few solutions are present in the literature for sub-1V continuous time analog filters design, but limited to hundreds of kHz bandwidth[9]. A possible solution for operating with large linearity, low power supply and large signal bandwidth is still represented

by the Active-g_m-RC biquadratic cell, with some design modification for low-voltage operation. This cell and, generally speaking, any Active-RC filters are dc-biased and then they operate with the opamp input and output common-mode voltages at the same level (V_{i_DC}= V_{o_DC}= V_{oa_DC}). Since in the standard cell I_l current source is not included, it will be neglected in the following discussion.
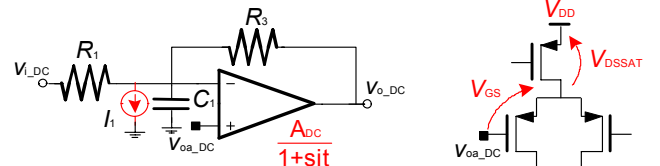

Fig. VIII - Active-Gm-RC cell and input diff pair bias point

Two conditions give the V_{DDmin} for proper operation:
- The filter input and output rail-to-rail swing requires:

$$V_{i\_DC}= V_{o\_DC} = V_{DDmin} / 2 \qquad (ii)$$

- The bias of the opamp input differential pair requires:

$$V_{oa\_DC}=V_{DDmin}-V_{GS}-V_{DSsat}= V_{DDmin} -V_{TH} -2 \cdot V_{ov} \qquad (iii)$$

Assembling the two equations, V_{DDmin} is given by:

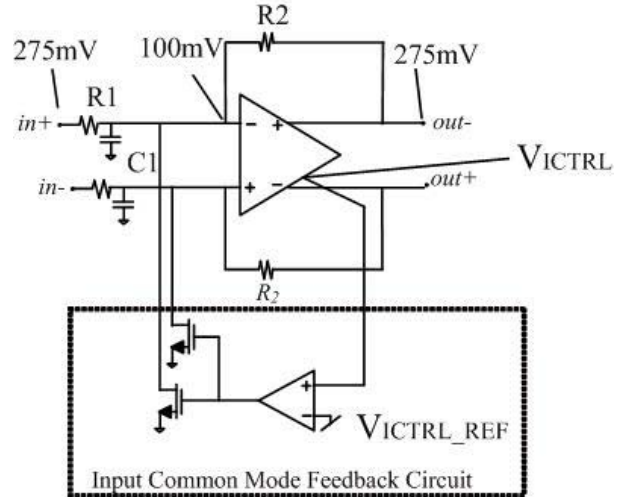$$V_{DDmin} = 2 \cdot V_{TH} + 4 \cdot V_{ov} \qquad (iv)$$
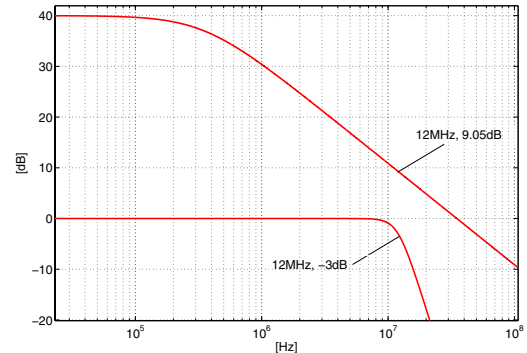

Fig. IX – Active Gm-RC Cell with I-CMFB

Fig. X – Opamp & Filter Transfer Function

For V_{TH}=300mV and V_{ov}=100mV, V_{DDmin}=1V results, too large for low-voltage applications. This requirement can be overcome by allowing a difference between V_{oa_DC} and $V_{i\_DC}= V_{o\_DC}$. Using a lower value for V_{oa_DC}, a lower V_{DDmin} is required. This is done by means of an Input-Common Mode Feedback circuit (I-CMFB), actuate by I_1, as shown in Fig. VIII. Regarding the input stage shown in the Fig. VIII, the V_{DDmin} as given in *(i)* is:

$$V_{DDmin} = 2 \cdot V_{ov} + V_{th} + V_{oa\_DC} + V_{in,swing} \qquad (v)$$

The above V_{DDmin} is reduced by introducing an I-CMFB, which forces V_{oa_DC} to a value lower than $V_{DD}/2$, while it maintains $V_{i\_DC}=V_{o\_DC}=V_{DDmin}/2$. The actuation of the I-CMFB control is done by means of two controlled current sources connected at the opamp input nodes as shown in Fig. IX. The opamp input dc voltage (V_{oa_DC}) has to be accurately evaluated in order to guarantee accurate operation of the MOS current source (i.e. $V_{oa\_DC} > V_{DSsat}$). This evaluation has to be done to the particular features of the Active-g_m-RC cell, used in this filter. At low frequency the large opamp gain guarantees the virtual ground principle and then no swing is present at the opamp input nodes. This means that at low frequency optimum bias can be designed. On the other hand, at high-frequency and, in particular, around the poles frequency, the virtual ground principle is not valid because in the Active-g_m-RC cell the opamp is used as open loop Integrator. Fig. X shos the opamp and the filter transfer functions. For a certain V_{ov} (typically $\approx$100mV), the maximum single ended output swing is $\pm V_{DD}/2 - V_{ov}$. So that considering the 9dB opamp gain at 12MHz and the -3dB filter attenuation at the same frequency, the input signal maximum swing is $(\pm V_{DD}/2 - V_{ov})/4$. From these considerations, for V_{DD}=550mV, the opamp input swing is about 45mV. Thus, since I_1 requires at least 50mV, the design gives V_{oa_DC}=100mV.

The I-CMFB circuit is composed by the single ended opamp and the current source. The opamp input nodes voltage depends on the resistances value and on the I_1 current flowing from the current source.

$$V_{oa\_DC} = \frac{V_{DD}}{2} - I_1 \cdot \frac{R_1 \cdot R_2}{R_1 + R_2} \qquad (vi)$$

So if the resistances value changes, as it happens in the reconfigurable filters, or for temperature reasons, then the Input CMFB regulates the I_1 value in order to maintain the V_{oa_DC} constant. The $V_{I\text{-}CTRL}$ common mode signal is sensed on the source node of the input differential pair MOS and compared with the reference value $V_{I\text{-}CTRL\_REF}$. The opamp schematic and the $V_{I\text{-}CTRL}$ node are shown in the Fig. XI .

At low supply voltage, cascode stages are not possible, and this decreases the achievable per-stage gain. In these conditions large opamp dc-gain can be obtained using multistage structures. A popular solution is the Miller-compensated two-stage opamp. The input stage is a differential pair and the output stage is a common source gain stage. Fig. XI shows the scheme of the opamp used in

this filter. This scheme allows optimizing opamp input stage and output stage features independently.
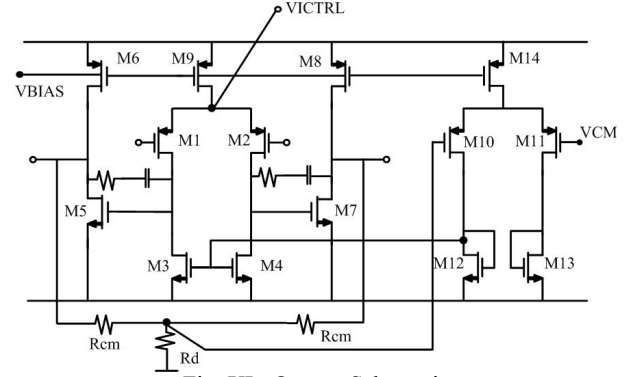

Fig. XI - Opamp Schematic

Regarding the output stage an Output Common-Mode-Feedback is used to maintain the output node voltage at $V_{DD}/2$. So also the input nodes of the Output CMFB opamp would have to be at $V_{DD}/2$, imposing the V_{DD} limitation of eq. *(i)*. To avoid this, a resistive partition and level shift branch composed by R_{cm}- R_d is used. This gives a slight reduction of the O-CMFB loop gain but allows reducing V_{DDmin} to:

$$V_{DD\,min} = \frac{V_{DD\,min}}{2} \cdot \frac{R_d}{R_d + R_{cm}/2} + V_{TH} + 2 \cdot V_{ov} \qquad (vii)$$
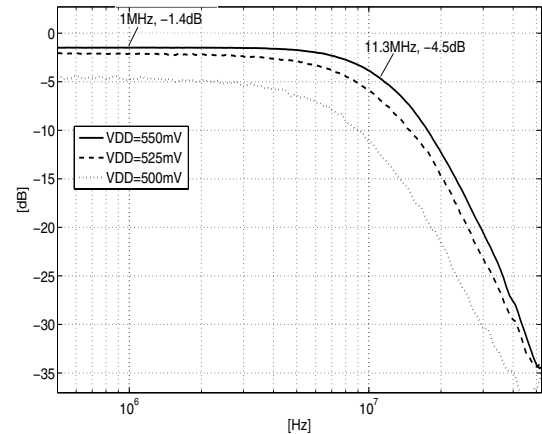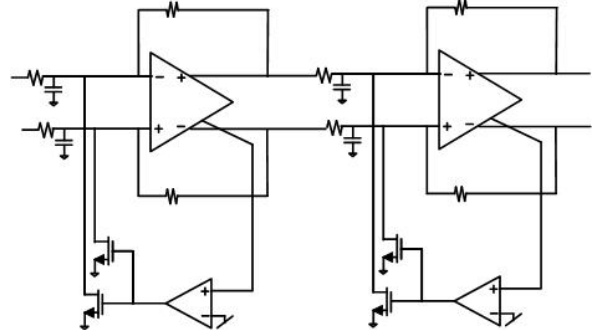

Fig. XII – 550mV WLAN Filter vs. VDD

Fig. XIII – 550mV supply Voltage WLAN Filter

Technology	0.13μm CMOS
Supply Voltage	0.55V
Die area occupation	0.45mm^2
Transfer Function	4th Order Butterworth
f_{3dB}	11.3MHz
Max f-3dB Deviation	4%
dc-gain	0dB
IRN	110μV$_{rms}$
In-band IIP3	8dBm
DR(THD=-40dBc)	60dB
Out-of-band IIP3	13.3dBm
Power Consumption	3.5mW

Tab. II – 550mV filter performance summary

Another negligible drawback is a slight output current increase to be fed to the resistive branch. The filter is optimized to operate at 550mV supply voltage. Fig. XII shows the filter frequency response. The overall top view is presented in the Fig. XIII. In the Tab. II gives the performance summary.

Fig. XIX shows the chip photo.

IV. A SOURCE-FOLLOWER-BASED FILTER

The source-follower is a well-known basic building block for CMOS designs. It, considering also its load capacitance, acts as a 1st-order low-pass filter and exhibits excellent linearity in particular with reduced overdrive voltages ($V_{ov}=V_{GS}-V_{TH}$). This is the opposite of other continuous-time filter implementations, where large linearity requires large V_{ov} and then large power for a given g_m ($g_m=2 \cdot I/V_{ov}$). In addition, the source follower exhibits other advantages:
• No parasitic poles, avoiding the power cost of pushing non-dominant singularities at high frequency.
• No common-mode feedback circuit (the output common-mode voltage is fixed by the transistors V_{GS}).
• Low-output impedance to drive following stages.

In [10] these source-follower features have been extended to the design of a 2nd-order low-pass filter and a 4th-order filter were designed by cascading two 2nd-order cells. The technique has been extended to the design of single-loop high-order source-follower-based continuous-time filters that, as for the ladder filters, would present lower frequency response sensitivity to component value variations. An efficient CMOS realization validates the proposal. It requires lower power and lower area with respect to other solutions. The filter architecture is based on the positive and negative 1st-order building blocks shown in Fig. XIV.
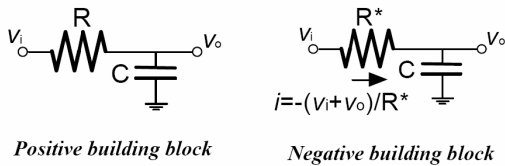

Fig. XIV – 1st order positive and negative building blocks

In the negative block, the small-signal voltage-to-current relationship of R* is:

$$i = -(v_i + v_o)/R \qquad (viii)$$

Composing a sequence of these cells allows synthesizing high-order filters. The sequence can be the regular alternation of positive and negative cells or they can be connected with a different order. A negative cell is needed to synthesize complex poles. In the following the regular alternation is considered and results in the generalized filter architecture of Fig. XV, whose general transfer function can be written as:

$$H(s)=\frac{1}{s^n \cdot R^n \cdot \prod_{1..n} C_i + s^{n-1} \cdot R^{n-1} \cdot \prod_{1..n-1} C_i +....+s \cdot R \cdot C_1 +1} \quad (ix)$$
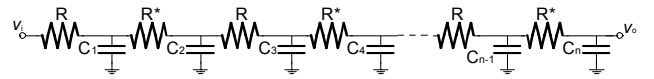

Fig. XV - The generalized filter architecture

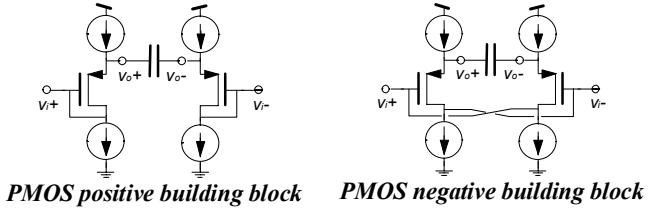PMOS positive building block   PMOS negative building block

Fig. XVI - Pseudo- differential PMOS positive and negative cells

This is the transfer function of a low-pass filter with unitary DC-gain. The advantage of this approach is significant in conjunction with the proposed efficient CMOS implementation shown in Fig. XVI for the positive and negative building blocks with PMOS devices (NMOS can also be considered). They are in pseudo-differential structure, as they will be in the final design. Designing a filter in this way guarantees to the structure the above advantages of the source follower. In addition, the generic time-constant is defined as:

$$\tau = \frac{C}{g_m} = \frac{C \cdot V_{ov}}{2 \cdot I} \qquad (x)$$

Due to large achievable g_m value (the linearity is proportional to g_m !), high-frequency filters (with small τ) can be realized using smaller value of capacitance, with significant area saving and die cost reduction.

A particular discussion regards the input stage. The overall filter can be built-up with the cells above presented. In this way, the input impedance depends on the input signal frequency. At low frequency the input impedance is equal to infinite (ideally) for an even-order structure. On the other hand, at high frequency for any filter order the input impedance is equal to R. If this impedance level is critical for the filter under development, just the first cell can be replaced by an ideal source-follower. In this case the input impedance is given by the source-follower input impedance that is quite large. The 2nd-order filter with a source follower

input stage built up with these cells corresponds to the scheme reported in [7].

The theoretical V_{DDmin} for these cells is:

$$V_{DDmin} = 3 \cdot V_{ov} + V_{TH} + V_{swing} \qquad (xi)$$

where V_{TH} is the threshold voltage while V_{swing} is the signal swing. A 6th-order low-pass filter prototype in a 0.13μm CMOS technology with V_{DD}=1.2V validates the proposal. The filter schematic is shown in.
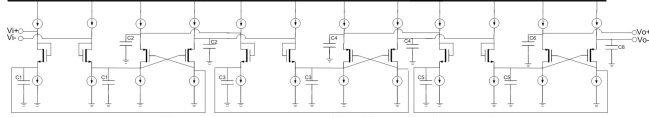

Fig. XVII – Overall Filter Schematic

The filter performance satisfies the requirements of the channel selection filter for a LDR-UWB receiver. The critical issue of source-follower-based cells (i.e. the dc voltage drop equal to V_{GS} between input and output nodes) is here solved by alternating NMOS and PMOS cells. In this way, the DC level is restored. Fig. XVIII shows the filter transfer function.
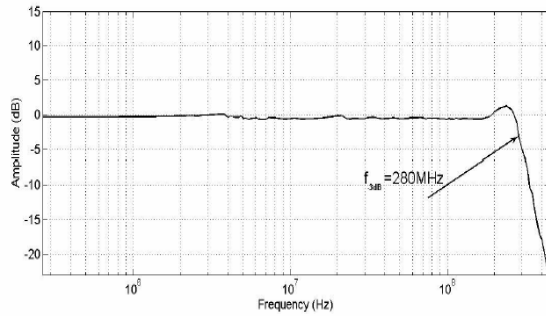

Fig. XVIII – Frequency Response

The cut-off frequency is 280MHz while the DC-gain is about 0dB. A 11dBm IIP3 have been measured. The output noise is about -140dBm@3MHz. The chip area occupation is as small as 200x90μm^2. In this filter the total amount of capacitance is 500fF, which occupies 0.01mm^2. On the other hand, the use of limited V_{ov}, allows to achieve large g_m with low current level. In this prototype, the total current is about 100μA for a total power supply of 120μW, which is favorable compared with the state of the art [10]. A performance resume of the filter presented in this section is reported in the Tab. III. Fig. XIX shows the chip photo.

Technology	0.13μm CMOS
Supply Voltage	1.2V
Die area occupation	0.018mm2
Transfer Function	-
f_{3dB}	280MHz
dc-gain	0dB
IRN	-140dBm@3MHz
In-band IIP3	11dBm
Power Consumption	0.12mW

Tab. III – Source Follower Based Filter Performance Resume
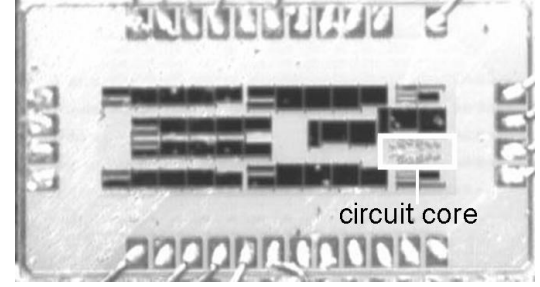

Fig. XIX – Source Follower Based Filter and 550mV WLAN Filter

V. CONCLUSIONS

In this paper three advanced solutions for low-power low-voltage circuits for telecom have been presented. These designed are strictly customized to different telecom standards. This allows a strong power consumption reduction. The Active-g_m-RC biquadratic cell exploits the frequency response of the opamp to synthesize a complex poles pair, reducing the unity gain bandwidth requirements of the opamp in the closed loop topologies. The second circuit is an interesting example of sub-1V analog circuits. A proper bias circuit is used to fix the operating point of the biquad. The third design exploits the source follower principle. Very low current consumption (100μA) is performed at 1.2V supply voltage in the 280MHz bandwidth.

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