A Logarithmic Full-Chip Thermal Analysis Algorithm Based on Multi-Layer Green's Function

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Abstract

This paper derives the multi-layer heat conduction Green's function, by integrating the eigen-expansion technique and the classic transmission line theories, and presents a logarithmic full-chip thermal analysis algorithm, which is verified by comparisons with a computational fluid dynamics tool (FLUENT). The paper considers Dirichlet's and general heat convection boundary conditions at chip surfaces. Experimental results show that the algorithm offers superior computing speed, compared to FLUENT and traditional Green's function based methods. The paper also studies the limitations of the traditional single-layer thermal model.

1. Introduction

Thermal issue is of paramount importance in chip performance and reliability modeling. Chip temperature variation may cause timing uncertainty and related failures by changing interconnect resistivity, may increase leakage power by super-linearly increasing gate sub-threshold current, and may shorten the mean time to fail of chip by worsening interconnect electromigration. Accurate thermal analysis is essential in a thermal-aware chip design flow [1].

Grid-based methods, e.g. finite-difference and finite-element methods, were successfully used in chip thermal analysis [2, 3]. They can be accelerated by model order reduction techniques [4, 5, 6]; however, grid-based methods are inefficient in an inner loop, such as in chip floorplanning and placement, compared to Green's function based approaches, which reduce thermal simulation time by orders of magnitude [7, 8, 9].

For thermal analysis, [10] considered Green's function for various boundary conditions (BCs) and uniform materials; [7] considered the free-space Green's function; [8], the multi-layer Green's function; and recently [9], the chip sidewalls. Green's function has frequently occurred in chip parasitics exaction (CPE) [11, 12, 13]. However thermal analysis differs from CPE. For example, in CPE, chip was often assumed horizontally infinite and vertically imposed with Neumann's BCs [13, 14]; however, in thermal analysis, chip need be considered horizontally finite and vertically imposed with heat convection BCs. Additionally, numerical stability problem can happen in calculating the same Green's function if different formulas are used [12, 15].

To accurately model a chip, horizontally finite and vertically consisting of layered materials, the paper derives the multi-layer heat conduction Green's function, by integrating the eigen-expansion technique and the classic transmission line theories. The paper offers a logarithmic algorithm, which significantly accelerates the full-chip thermal analysis, compared to traditional Green's function based methods, which are of quadratic complexity and resemble a matrix-vector product procedure [7, 8, 9].

The rest of the paper is organized as follows. Section 2 mathematically describes the chip thermal analysis issue. Section 3 derives the multi-layer heat conduction Green's function. Section 4 introduces a logarithmic thermal analysis algorithm. Section 5 experimentally demonstrates the accuracy and scalability of the algorithm and discusses the limitations of the traditional single-layer thermal model.

2. Full-chip thermal analysis based on Green's function

Given a chip, described by the multi-layer thermal model (MLTM) in Fig.1(a), its steady-state temperature distribution is determined by the 3-D heat conduction equation, written in Cartesian coordinates as

$$\nabla \cdot [\nabla k(z) T(x,y,z)] = -f(x,y,z), \tag{1}$$

where T denotes temperature (in kelvin, or K); f, heat source power density (in W/m^3); and k, material thermal conductivity (in W/(m K)). k is only z-axis dependent, with $k(z) = k_m$, for $z_{m-1} < z < z_m$ and $1 \le m \le n$.

In addition, there are two sets of heat conduction boundary conditions (BCs) specified for the chip: sidewall BCs and inter-layer BCs.

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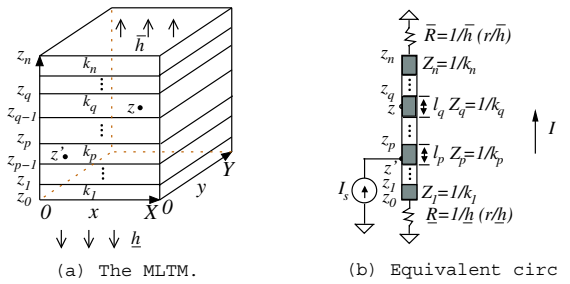


Figure 1. The MLTM and the equivalent circuit for computing Green's function.

a). Sidewall BCs: The four chip sidewalls are approximately insulated from the ambient, thereby specified with Neumann's BCs, i.e. $\frac{\partial T}{\partial x}\Big|_{x=0,X}=0$ and $\frac{\partial T}{\partial y}\Big|_{y=0,Y}=0$, where X and Y denote the chip $x-y$ dimensions.

b). Inter-layer BCs: At inner interface z_m, for $0<m<n$, BCs are specified to describe the continuity of temperature, i.e. $T(x,y,z_{m+})=T(x,y,z_{m-})$ and the continuity of heat flux through the interface, i.e. $k(z_m+)\frac{\partial T}{\partial z}\Big|_{z=z_m+}=k(z_m-)\frac{\partial T}{\partial z}\Big|_{z=z_m-}$; and at the chip top and bottom faces, heat convection BCs are specified:

$$k_1\frac{\partial T}{\partial z}\Big|_{z=z_0}=\underline{h}T \text{ and } -k_n\frac{\partial T}{\partial z}\Big|_{z=z_n}=\bar{h}T,$$

where $\underline{h}$ (or $\bar{h}$) is the heat transfer rate from the bottom (or top) face z_0 (or z_n) to the ambient, with units W/(m^2 K). The paper chooses the ambient temperature as the reference.

Heat conduction Green's function $G(x,y,z|x',y',z')$, i.e. the Green's function of (1), corresponds to the chip temperature distribution caused by a Dirac delta source $\delta(x-x',y-y',z-z')$ at chip location (x',y',z'). It satisfies

$$\nabla\cdot[\nabla k(z)G(x,y,z|x',y',z')]=-\delta(x-x',y-y',z-z') \qquad (2)$$

and the sidewall and inter-layer BCs, in which T need be replaced by G. Given $G(x,y,z|x',y',z')$, the chip temperature distribution can be represented by a spatial convolution:

$$T(x,y,z)=\int_{\mathcal{V}}G(x,y,z|x',y',z')f(x',y',z')dx'dy'dz', \qquad (3)$$

where $\mathcal{V}$ denotes the entire volume space of the given chip.

The following section will detail the derivation of the heat conduction Green's function for 3-D layered chips.

3. Deriving heat conduction Green's function

After extended from space $\mathcal{V}$ to the entire 3-D space as an even and periodic function of x of period $2X$, as well as an even and periodic function of y of period $2Y$, heat conduction Green's function has an eigen-expansion:

$$G(x,y,z|x',y',z')=\sum_{i=0}^{\infty}\sum_{j=0}^{\infty}\phi_{ij}(x,y)G_{ij}(z|x',y',z'), \qquad (4)$$

where eigenfunction $\phi_{ij}(x,y)=\cos\left(\frac{i\pi x}{X}\right)\cos\left(\frac{j\pi y}{Y}\right)$. Eigen-expansion (4) ensures G satisfies the sidewall BCs.

Similarly, the 3-D delta function has an eigen-expansion:

$$\delta(x-x',y-y',z-z')=\sum_{i=0}^{\infty}\sum_{j=0}^{\infty}c_{ij}\phi_{ij}(x,y)\phi_{ij}(x',y')\delta(z-z'), \qquad (5)$$

where $c_{ij}=2^d/XY$ and d is the dimensionality of ϕ_{ij}: $d=0,1,2$ for the three cases that both i and j are zero, only one of them is zero, and none of them is zero.

Insert (4) and (5) into (2). Then G_{ij} satisfies

$$\frac{\partial^2 G_{ij}}{\partial z^2}-\gamma_{ij}^2G_{ij}=-\frac{1}{k(z)}c_{ij}\phi_{ij}(x',y')\delta(z-z'), \qquad (6)$$

where $\gamma_{ij}=\sqrt{\frac{i^2\pi^2}{X^2}+\frac{j^2\pi^2}{Y^2}}$. To solve G_{ij} from (6), the paper employs the classic transmission line theories.

3.1. Eigen-expansion coefficient G_{ij} ($i=j=0$)

Consider (6). When $i=j=0$, γ_{ij} becomes 0. To compute G_{00}, the paper constructs a circuit consisting of an n-section line conductor of per unit-length (PUL) conductance $k(z)$. The line has a current source input I_s of intensity $c_{00}\phi_{00}(x',y')$ at location z' and has its two ends terminated by two resistors of resistances $\underline{R}=1/\underline{h}$ and $\bar{R}=1/\bar{h}$, as shown in Fig.1(b).

Compare (6) with the line conductor circuit equations $\frac{\partial V(z)}{\partial z}=-\frac{I(z)}{k(z)}$ and $\frac{\partial^2 V(z)}{\partial z^2}=-\frac{I_s}{k(z)}\delta(z-z')$, and also heat conduction BCs with circuit equations at line section boundaries. It is clear that G_{00} corresponds to the voltage at location z in the line conductor. Hence,

$$G_{00}(z|x',y',z')=c_{00}\phi_{00}(x',y')H_{00}(z|z'), \qquad (7)$$

where H_{00} is the line transfer impedance from source z' to target z. According to Fig.1(b), assuming that source z' is in layer p and target z is in layer q, H_{00} is derived:

$$H_{00}(z|z')=\frac{\left[\underline{Z}_p+Z_p(z'-z_{p-1})\right]\left[\bar{Z}_q+Z_q(z_q-z)\right]}{\underline{Z}_p+Z_pl_p+\bar{Z}_q}. \qquad (8)$$

In the paper, for the m-th line section, $\underline{Z}_m$ denotes the input impedance seen from its bottom boundary toward the bottom end of the entire circuit, $\bar{Z}_m$ denotes the input impedance seen from its top boundary toward the top end of the entire circuit, Z_m denotes its characteristic impedance with $Z_m=1/k_m$, and l_m is its length.

3.2. Eigen-expansion coefficient G_{ij} $(i+j>0)$

When $i+j>0$, an equivalent transmission line (TL) circuit can be constructed. Compare (6) to TL equations $\frac{\partial V}{\partial z}=-(R+sL)I$ and $\frac{\partial I}{\partial z}=-(G+sC)V+I_s\delta(z-z')$, or in the form of $\frac{\partial^2 V}{\partial z^2}-\gamma^2 V=-\gamma Z I_s\delta(z-z')$, where γ is the TL propagation constant given by $\gamma=\sqrt{(R+sL)(G+sC)}$, and Z is the characteristic impedance given by $Z=\sqrt{(R+sL)/(G+sC)}$. Evidently, G_{ij} corresponds to the voltage at location z in an n-section nonuniform TL of $\gamma=\gamma_{ij}$ and $Z=1/k(z)$, with a current source input $I_s=\frac{c_{ij}}{\gamma_{ij}}\phi_{ij}(x',y')$ at location z'. For the m-th TL section, its PUL parameters satisfy $\sqrt{RG}=\gamma_{ij}$, $\sqrt{R/G}=Z_m=1/k_m$, and $L=C=0$. The two ends of the TL are terminated by two resistors: $\underline{R}=\gamma/\underline{h}$ and $\bar{R}=\gamma/\bar{h}$. The equivalent circuit is illustrated by Fig.1(b) as well.

Based on the figure, G_{ij} is derived and given by

$$G_{ij}(z|x',y',z')=c_{ij}\phi_{ij}(x',y')H_{ij}(z|z'), \tag{9}$$

where H_{ij} is the normalized TL transfer impedance from location z' to location z by propagation constant γ, with $\gamma=\sqrt{\frac{i^2\pi^2}{X^2}+\frac{j^2\pi^2}{Y^2}}$. Assuming that source z' is in layer p and target z is in layer q, H_{ij} is derived as the following:

$$H_{ij}(z|z')=\frac{\xi(\underline{Z}_p\cosh\gamma\underline{l}+Z_p\sinh\gamma\underline{l})(\bar{Z}_q\cosh\gamma\bar{l}+Z_q\sinh\gamma\bar{l})}{Z_p(\underline{Z}_p+\bar{Z}_p)\cosh\gamma l_p+(Z_p^2+\underline{Z}_p\bar{Z}_p)\sinh\gamma l_p}, \tag{10}$$

where $\underline{l}=z'-z_{p-1}$, $\bar{l}=z_q-z$, and ξ is given by

$$\xi=\frac{Z_p\prod_{m=p}^{q-1}\bar{Z}_m}{\gamma\prod_{m=p+1}^{q}(\bar{Z}_m\cosh\gamma l_m+Z_m\sinh\gamma l_m)}.$$

Input impedances $\underline{Z}$'s or $\bar{Z}$'s have recurrence formulas: for one TL section, its input impedance at its one boundary, Z_{in} is given by $Z_{in}=ZC\frac{ZL+ZC\tanh\gamma L}{ZC+ZL\tanh\gamma L}$, where ZL is the load impedance at its other boundary; ZC, the section characteristic impedance; and L, the section length.

The paper has derived closed formulas for the multi-layer heat conduction Green's function, by integrating the eigen-expansion technique and the classic transmission line theories. For other types of sidewall BCs than Neumann's BCs, the previous derivation can still be applied. For example, if Dirichlet BCs are imposed on chip sidewalls, i.e. assume the sidewall temperatures are same as the ambient, G_{ij} can be obtained by following the previous derivation, after changing the eigenfunction to $\phi_{ij}(x,y)=\sin\left(\frac{i\pi x}{X}\right)\sin\left(\frac{j\pi y}{Y}\right)$. In addition, relating G_{ij} to circuit transfer functions in the closed formulas can overcome numerical problems. For example, when heat transfer rate $\underline{h}$ or $\bar{h}$ is zero or closed to zero, the loading impedances for the equivalent circuits become infinite or extremely large; therefore, instead of using impedance formulations, using admittance formulations for G_{ij} can avoid numerical overflows.

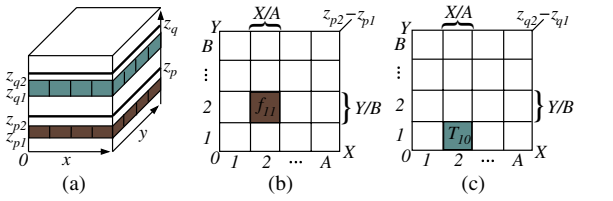


Figure 2. Heat source model: (a) source and target regions $z\in[z_{p1},z_{p2}]$ and $z\in[z_{q1},z_{q2}]$; (b) and (c) discretization of source and target layers.

4. A logarithmic thermal analysis algorithm

Based on the derived multi-layer heat conduction Green's function, this section introduces a logarithmic algorithm for full-chip thermal analysis.

Consider the heat source model. The paper discretizes the heat sources in a layer, e.g. the p-th layer, into $A\times B$ uniform cells, each being $\frac{X}{A}\times\frac{Y}{B}\times(z_{p2}-z_{p1})$ and having a uniform power density, as shown in Fig.2(a) and (b). In a given layer, the paper names cell (a,b) after the cell that is the $(a+1)$-th in the x direction and the $(b+1)$-th in the y direction, where $0\le a\le A-1$ and $0\le b\le B-1$. For cell (a,b), its power density is denoted by f_{ab}, and its temperature is denoted by T_{ab}.

The temperature distribution of a given target layer, e.g. layer q, can be obtained by superposing the temperature distribution raised by each layer of heat sources. Therefore, the paper considers the evaluation of temperature distribution at layer q, raised by the heat sources at a single layer, e.g. layer p. Target layer q is illustrated in Fig.2(a) and (c). To compute the temperature distribution in layer q caused by heat source layer p, traditional Green's function based methods used a simple matrix-vector product like procedure and required $O\left(A^2B^2\right)$ computations [7, 8, 9]. Compared to traditional methods, the algorithm presented in the following is of logarithmic complexity $O(AB\log(AB))$.

4.1. Temperature distribution caused by layer p

Refer to Fig.2(b). Insert eigen-expansion (4) into (3) and integrate with heat source power densities for layer p. Then the temperature at location (x,y,z), $T(x,y,z)$ is derived:

$$\begin{aligned}T(x,y,z)&=\sum_{i=0}^{\infty}\sum_{j=0}^{\infty}c_{ij}\phi_{ij}(x,y)\cdot\\&\int_0^X\int_0^Y\int_{z_{p1}}^{z_{p2}}\phi_{ij}(x',y')H_{ij}(z|z')f(x',y',z')dx'dy'dz'\\&=\sum_{i=0}^{\infty}\sum_{j=0}^{\infty}\frac{2^d\sin\frac{i\pi}{2A}\sin\frac{j\pi}{2B}}{ij\pi^2}F_{ij}\phi_{ij}(x,y)\int_{z_{p1}}^{z_{p2}}H_{ij}(z|z')dz',\end{aligned} \tag{11}$$

where

$$F_{ij} = \int_0^X \int_0^Y \frac{ij\pi^2}{XY} \csc\frac{i\pi}{2A} \csc\frac{j\pi}{2B} \phi_{ij}(x',y') f(x',y',z') dx'dy' = \sum_{a=0}^{A-1}\sum_{b=0}^{B-1} 4 f_{ab} \cos\frac{i\pi(2a+1)}{2A} \cos\frac{j\pi(2b+1)}{2B}. \quad (12)$$

F_{ij} is the two-dimensional discrete cosine transform (2-D DCT) of f_{ab}. Therefore all F_{ij}, for $0 \le i \le A-1$ and $0 \le j \le B-1$, can be computed in $O(AB\log(AB))$. For i, j outside that range, by exploiting the periodicity of F_{ij}, the required values can be conveniently obtained.

4.2. A logarithmic thermal analysis algorithm

Refer to Fig.2(c). For cell (a,b) in target layer q, its average temperature T_{ab} can be obtained by integrating $T(x,y,z)$ in (11) over cell (a,b):

$$T_{ab} = \sum_{i=0}^{\infty}\sum_{j=0}^{\infty} F_{ij} \frac{2^d AB \sin\frac{i\pi}{2A} \sin\frac{j\pi}{2B}}{ijXY\pi^2(z_{q2}-z_{q1})} \int_{z_{q1}}^{z_{q2}} \int_{z_{p1}}^{z_{p2}} H_{ij}(z|z')dz'dz \cdot \int_{aX/A}^{(a+1)X/A} \int_{bX/B}^{(b+1)X/B} \phi_{ij}(x,y)dxdy = \sum_{i=0}^{\infty}\sum_{j=0}^{\infty} 2^{d-2} F_{ij} IH_{ij} \cos\frac{i\pi(2a+1)}{2A} \cos\frac{j\pi(2b+1)}{2B}, \quad (13)$$

where IH_{ij} is given by

$$IH_{ij} = \frac{16AB\sin^2\frac{i\pi}{2A}\sin^2\frac{j\pi}{2B}}{i^2j^2\pi^4(z_{q2}-z_{q1})} \int_{z_{q1}}^{z_{q2}} \int_{z_{p1}}^{z_{p2}} H_{ij}(z|z')dz'dz. \quad (14)$$

Then the series representation of T_{ab} in (13) is truncated:

$$T_{ab} \approx \sum_{i=0}^{A-1}\sum_{j=0}^{B-1} 2^{d-2} F_{ij} IH_{ij} \cos\frac{i\pi(2a+1)}{2A} \cos\frac{j\pi(2b+1)}{2B}, \quad (15)$$

which is the two-dimensional inverse discrete cosine transform (2-D IDCT) of $F_{ij}IH_{ij}$. Note that to improve accuracy, higher order coefficients $F_{ij}IH_{ij}$ can be added to their lower order companions, by exploiting the periodicity of $\cos\frac{i\pi(2a+1)}{2A}\cos\frac{j\pi(2b+1)}{2B}$; however, later experiments show that (15) is already sufficiently accurate.

Based on (12) and (15), a logarithmic algorithm is proposed for computing the temperature at layer q caused by heat sources in layer p. The algorithm is in $O(AB\log(AB))$ and shown in Fig.3.

4.3. The pre-characterization of IH_{ij}

For a given chip, IH_{ij}'s need be pre-characterized only once. The following details the computing of IH_{ij}. Let $\hat{H}_{ij}$ denote the integral term in (14), i.e. $\hat{H}_{ij} = \int_{z_{q1}}^{z_{q2}} \int_{z_{p1}}^{z_{p2}} H_{ij}(z|z')dz'dz$. Note that for H_{ij} given in (8) and (10), the paper has assumed that either layer p is lower than layer q, or both $p = q$ and $z' < z$. When the assumption is not satisfied, H_{ij} can be obtained by exploiting the reciprocity of transfer impedances: if $p = q$ and $z' > z$, H_{ij} can be obtained by exchanging z and z' in (8) and (10); otherwise, if $p > q$, H_{ij} can be obtained by exchanging subscripts p and q, as well as z and z' in (8) and (10). Therefore the paper considers three cases.

Begin

1. Compute IH_{ij}'s based on (14) if they are not pre-calculated. In pre-calculating IH_{ij}, (16) and (17) need be used.
2. Given one layer of heat sources, whose power densities form a 2-D array made of f_{ab}'s, compute the 2-D DCT of f_{ab} to obtain F_{ij}, based on (12).
3. Form an array made of $F_{ij}IH_{ij}$, then compute the array's 2-D IDCT to obtain T_{ab}, based on(15).

End

Figure 3. The logarithmic chip-level thermal analysis algorithm.

a). The case $p = q$: From (8) and (10), $\hat{H}_{ij}$ is obtained as follows:

$$\hat{H_{ij}} = \begin{cases} \alpha l_{pv}^2 \left[\left(\frac{\underline{Z}_p}{Z_p} + \frac{2z_{p1}+z_{p2}}{3} - z_{p-1}\right) \cdot \left(\frac{\bar{Z}_q}{Z_q} + z_q - \frac{2z_{q2}+z_{q1}}{3}\right) - \frac{l_{qv}^2}{36}\right] & i=j=0 \\ \left[\underline{D}_{ij}(e^{-\gamma l_{2c}} - e^{-\gamma l_{1c}})^2 + \bar{D}_{ij}(e^{\gamma l_{1c}} - e^{\gamma l_{2c}})^2 + 2\underline{D}_{ij}\bar{D}_{ij}e^{-\gamma l_q}\left(e^{\gamma l_{qv}} - \gamma l_{qv} - 1\right) + 2e^{\gamma l_p}\left(e^{-\gamma l_{pv}} + \gamma l_{pv} - 1\right)\right] E_{ij}, & i+j>0 \end{cases} \quad (16)$$

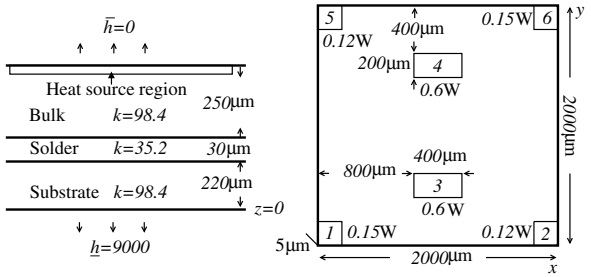
where $l_{1c} = z_{p1} - \frac{z_p + z_{p-1}}{2}$, $l_{2c} = z_{p2} - \frac{z_p + z_{p-1}}{2}$, $l_{pv} = z_{p2} - z_{p1}$, and $l_{qv} = z_{q2} - z_{q1}$.

b). The case $p < q$: From (8) and (10), $\hat{H}_{ij}$ is obtained:

$$\hat{H}_{ij} = \begin{cases} \alpha l_{pv} l_{qv} \left(\frac{\underline{Z}_p}{Z_p} + \frac{z_{p1}+z_{p2}}{2} - z_{p-1}\right) \cdot \left(\frac{\bar{Z}_q}{Z_q} + z_q - \frac{z_{q1}+z_{q2}}{2}\right) & i=j=0 \\ E_{ij}\left[\underline{D}_{ij}(e^{-\gamma \underline{l}_{p1}} - e^{-\gamma \underline{l}_{p2}}) + e^{\gamma \underline{l}_{p2}} - e^{\gamma \underline{l}_{p1}}\right] \cdot \left[\bar{D}_{ij}(e^{-\gamma \bar{l}_{q2}} - e^{-\gamma \bar{l}_{q1}}) + e^{\gamma \bar{l}_{q1}} - e^{\gamma \bar{l}_{q2}}\right] & i+j>0 \end{cases} \quad (17)$$

where $\underline{l}_{p1,2} = z_{p1,2} - z_{p-1}$ and $\bar{l}_{q1,2} = z_q - z_{q1,2}$.

c). The case $p > q$: $\hat{H}_{ij}$ is similar to (17). $\hat{H}_{ij}$ can be obtained by exchanging the subscripts p and q in (17), as well



(a) Chip thermal profile. (b) Heat source placement.

Figure 4. The simulated 3-layer chip example.

as p and q in the coefficients α, $\underline{D}_{ij}$, $\bar{D}_{ij}$, and E_{ij}, where

$$\alpha = \frac{Z_p Z_q}{\underline{Z}_p + Z_p l_p + \bar{Z}_q},$$

$$\underline{D}_{ij} = \frac{\underline{Z}_p - Z_p}{\underline{Z}_p + Z_p}, \quad \bar{D}_{ij} = \frac{\bar{Z}_q - Z_q}{\bar{Z}_q + Z_q},$$

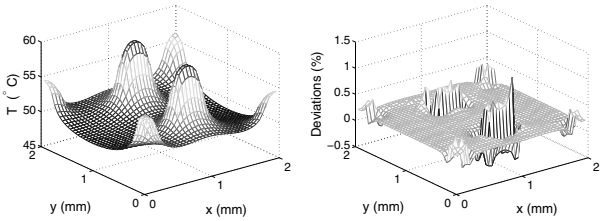
$$E_{ij} = \frac{\chi_{pq}}{4\gamma^2} \frac{(\underline{Z}_p + Z_p)(\bar{Z}_q + Z_q)}{Z_p(\underline{Z}_p + \bar{Z}_p)\cosh\gamma l_p + (Z_p^2 + \underline{Z}_p \bar{Z}_p)\sinh\gamma l_p}.$$

According to Fig.1(b), $\underline{D}_{ij}$ is the reflection coefficient of the p-th TL section, seen from its bottom boundary toward the bottom end of the entire circuit, and $\bar{D}_{ij}$ is the reflection coefficient of the q-th TL section, seen from its top boundary toward the top end of the entire circuit. Since the coefficients $\underline{D}_{ij}$, $\bar{D}_{ij}$, and E_{ij} depend upon only a single parameter γ, they can be pre-characterized into one-dimensional lookup tables to facilitate the pre-characterization of IH_{ij}.

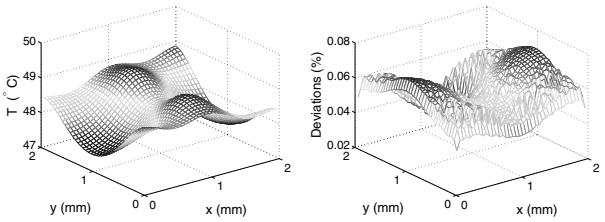
5. Experimental results

The logarithmic algorithm shown in Fig.3 has been verified by comparisons with a computational fluid dynamics tool (FLUENT). Fig.4(a) shows a simulated chip example of three layers. The top heat transfer rate $\bar{h} = 0$, and the bottom heat transfer rate $\underline{h} = 9000$ W/(m^2 K). Six heat sources are in the 5 μm thick heat source region, and the position and the power of each heat source are in Fig.4(b).

In using the algorithm, A and B were set to 40. However it is recommended that A and B be the powers of 2, to facilitate the DCT/IDCT. The results are shown in Fig.5, where the left graphs give the temperature distributions obtained from the algorithm, and the right graphs show the relative temperature differences from FLUENT in percentages. The temperature deviations between the two methods are within 1.13% for the heat source region and within 0.07% for the chip bottom. The pre-characterization of IH_{ij} took 1.265 s, and temperature evaluation after pre-characterization took only 8 ms; however, using FLUENT took 112 s to obtain the temperature distribution. The CPU usages were taken from a SUN Blade 1500 machine. Note that in practice, A and B can be doubled to verify the convergence of the algorithm.

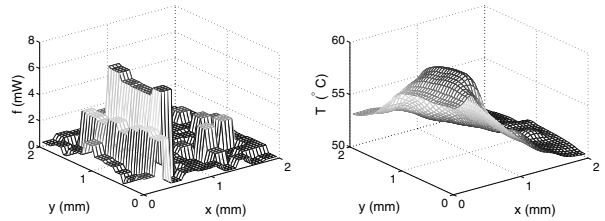


(a) Heat source region temperature and temperature deviation.



(b) Chip bottom temperature and temperature deviation.

Figure 5. Comparisons between the algorithm and FLUENT.



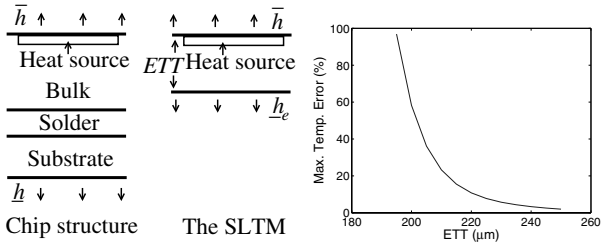
(a) Power density distribution f. (b) Heat source region temperature.

A, B	$40, 40$	$40, 80$	$80, 80$	$80, 120$	$120, 120$
Log. (ms)	4	6	10	15	24
Trad. (ms)	29	113	487	1554	3480

Figure 6. Scalability of the proposed algorithm.

5.1. Scalability of the proposed algorithm

Fig.6 shows the calculated heat source region temperature distribution by the proposed algorithm, for the chip in Fig.4(a), under a randomly generated power density function f. For comparison, a simple matrix-vector product procedure was implemented to simulate the traditional methods [7, 8, 9], The table in Fig.6 shows the CPU usages of the proposed algorithm (excluding the time for pre-characterization, as it need be done only once) and the traditional methods, when $A \times B$ was increased from 40×40 to 120×120. Evidently, the proposed algorithm has superior speed due to its logarithmic complexity, compared to the traditional methods, whose complexities are quadratic.



(a) Single-layer thermal model. (b) Accuracy of SLTM versus ETT.

Figure 7. Single-layer thermal model, and its accuracy versus effective thermal thickness.

5.2. Limitations of the single-layer thermal model

Traditionally, a single-layer thermal model (SLTM) was used to describe a multi-layer chip [7, 9]. Fig.7(a) shows such a single-layer thermal model, where $\underline{h}_e$ is the effective heat transfer rate that can be determined by the approach in [2], and ETT is named the effective thermal thickness.

Using the chip in Fig.4, the paper employed the proposed algorithm to analyze the average temperature distribution of the heat source region, by using the SLTM. Fig.7(b) plots the maximum errors of the calculated temperature distribution based on the SLTM, when ETT was varied. The figure shows that the accuracy of the SLTM was very sensitive to ETT. For the chip in Fig.4, to ensure the temperature errors within 1.97%, both the bulk and solder regions need be modeled, which is, however, beyond the capability of the SLTM. Hence, there are obstacles in using the SLTM for 3-D ICs [16].

6. Conclusions

By integrating the eigen-expansion technique and the transmission line theories, the paper derived the multi-layer heat conduction Green's function, based on which a logarithmic full-chip thermal analysis algorithm was introduced. Experiments demonstrated that the algorithm was very accurate and well-scalable, compared to FLUENT and traditional Green's function based methods. In addition, the paper discussed the limitations of the traditional single-layer thermal model.

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