Analysis and Modeling of Power Grid Transmission lines

J.Balachandran, S.Brebels, G.Carchon, T.Webers, W.De Raedt, B.Nauwelaers [(1)] and E.Beyne
Microwave and RF Systems Group, IMEC vzw, Kapeldreef 75, 3001, Leuven, Belgium
[(1)] Katholieke Universiteit Leuven, ESAT, Kasteelpark Arenberg 10, 3001 Leuven, Belgium.
Phone: +32 16 288700 Fax: +32 16 281501 e-mail: bchandra@imec.be

Abstract

Power distribution and signal transmission are becoming key limiters for chip performance in nanometer era. These issues can be simultaneously addressed by designing transmission lines in power grids. The transmission lines are well suited for high quality intra-chip signal transmission at multi gigabit data rates. By having signal lines between the power grids, the VDD and GND lines in the grid can be exploited as return paths besides being used for regular power distribution. This approach also improves wiring density. In this paper, we rigorously analyze and discuss the design considerations for laying transmission lines in power grids. We also present design oriented modeling methods in 2D and 3D geometry. We show how the grid modeling complexity is simplified. We experimentally validate our results with fabricated test structures. We also show VDD lines in the grid act as good return path without external decoupling capacitors in our design. Further we discuss substrate effects and deduce guidelines for designing power grid transmission lines on a low resistive silicon substrate.

I. Introduction

As the semiconductor technology steps into nanometer era, chip design is becoming ever challenging and complicated. ITRS roadmap [1] projects integration densities on the order of billion transistors in advanced nano technology nodes. This explosion in transistor counts enables more functional units for the same die area. Not only integration capacity went up but also the chip operating frequencies moved to microwave (*GHz*) range. This evolution makes communication instead of computation a bottleneck: ability to communicate over such large number of functional blocks at high speeds. Specifically the communication problem is due to interconnect that wires the functional blocks together - global interconnects as they are called. While transistor performance improves with scaling, interconnect deteoriates. As a result, communication bandwidth and latencies are severely constrained. Furthermore, power/energy per communication bit has also increased dramatically.

In addition to the global interconnect delay, power distribution within the chip is becoming detrimental to the overall performance in nanometer regime. With scaling, supply voltage (VDD) is reduced to bring down power requirements. However, exponential increase in number of transistors tends to offset scaling induced power reduction by keeping it either constant or even worsening. As a result, there is an unprecedented increase in supply current (I_{dd}). ITRS road map [1] projects current drain in the range of 360A at 35nm technology node. Consequently, even a small resistance of the power distribution network can lead to significant voltage drop, hurting the performance.

The power distribution and global interconnect issues can be simultaneously addressed by designing LC transmission lines in power grids. The (LC) transmission lines are well suited for high quality intra-chip signal transmission at multi gigabit data rates. In [2] it was shown that transmission lines compared to conventional global (RC) interconnects offer superior bandwidth, latency and power characteristics. Benefits of transmission lines for on-chip cache applications are discussed in [3]. By having signal lines between the power grids, the VDD and GND lines in the grid can be exploited as current return paths besides being used for regular power distribution.

However a disadvantage of the transmission line approach is it's poor wiring density [2, 3]. The transmission lines not only require fat metal wires but also need good return paths. These return paths contribute significantly to reduction in wiring density. For instance, a microstrip transmission line uses a dedicated ground plane while CPW configuration uses wide ground lines on either side of the signal line. Alternatively instead of dedicated return path structures, VDD (PWR) and GND lines in the power grid can be effectively used as current returns by careful design. In [4] design of signal lines with grid lines as return path is limited to reducing inductive effects. [5] discusses the advantages of signal lines in a fabric of power and ground lines but only in the context of conventional RC lines. In this paper, we present design oriented modeling methods and analyze the transmission lines in power grids in detail. We also experimentally validate our results.

II. Review of Power Grid structures

One of the important goals of any power grid structure is to have sufficiently low power supply impedance to avoid unacceptable voltage drops on the grid. Lower power grid impedance is achieved by lower resistance, inductance and larger capacitance. Fig 1 shows the different types of grid configurations. In Fig. 1a, PWR and GND lines occupy two different layers and are non-interdigitated. In Fig 1b, power lines fill one half of the grid and the ground lines fills the other half. In Fig.1c, PWR and GND lines are interdigitated

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and equipotential lines across the layers are connected through vias. All these structures essentially have same order of resistances and capacitances but the interdigitated structure in Fig 1c, offers the lowest grid inductance [6]. This is the grid structure of interest in this work and considered for all subsequent analysis. In between the interdigitated power and ground lines, a signal line is routed.

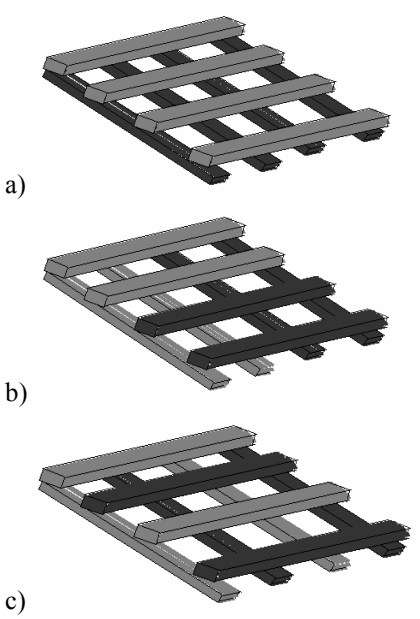

Fig 1. Different Power grid configurations. GND lines are marked in black while PWR lines are shown in grey.

III. Design Considerations for power grid Transmission lines

The design parameters of a power grid transmission line are shown in fig 2. In order for the propagating wave not to sense the influence of discontinuities (caused by orthogonal lines in the layers above or below), Grid Pitch (GP = W_p + GS) should be well below the wavelength of the highest frequency wave under propagation. For a signal propagating with a rise time T_r, the GP can be expressed as

$$GP << \frac{2T_r c_0}{\sqrt{\varepsilon_r}} \qquad (1)$$

Where c_o is the speed of light in vacuum and ε_r is the relative dielectric constant. Smaller values of GS helps to reduce power grid impedance with good inherent decoupling capacitance formed between PWR and GND lines. However smaller values of GS lowers the wiring density, otherwise available for signal routing. Thus the lower limit of GS is determined by the desired signal wiring density and upper limit is determined from eqn. 1.

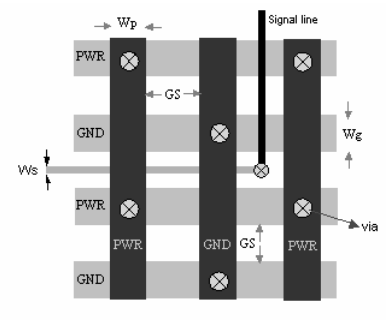

Fig 2. Design parameters of transmission line in Power Grid

For the PWR line also to act as good path (thereby reducing losses and cross-talk), it should have adequately small impedance to the GND line. The lower impedance to the GND can be achieved using external decoupling capacitors. Alternatively, inherent decoupling capacitance formed between PWR and GND lines can also be exploited to lower PWR-GND impedance.

While the width of signal line in the power grid is inversely proportional to the characteristic impedance (Z0), the width of PWR and GND lines has no significant impact on Z0. However their width controls the DC and high frequency losses, and hence the transmission line bandwidth. The minimum width of the PWR and GND lines is determined from supply current density requirements on the grid.

IV Modeling Methods

In this section, we discuss design oriented modeling methods for transmission lines in power grids. By design-oriented model, we mean a model for predicting transmission line parameters such as Z0 and RLGC line parameters. Analytical modeling is not suitable for this work because of complex multi layer geometry. The best option is to input geometry and material properties on to an EM field solver. The EM field solver may directly provide RLGC line parameters or S-parameter matrix from which these parameters can be extracted. These values are then corroborated with experimental results. However, the EM field solving in general is computationally expensive and resource intensive. The crux lies in specifying simplified geometry for EM field solving yet obtain results with sufficient accuracy. For instance, transmission lines with uniform cross sections such as microstrip and CPW, it is sufficient to simulate the *2D* cross section, which yields faster, and accurate results. However, power grid structures are inherently *3D* in nature because of the orthogonal 'overhead' lines in the adjacent layers. Alternatively, on a *3D* EM field solver, simulating a manageable small segment of transmission line is sufficient for uniform transmission line configurations such as Microstrip and CPW. Although power grid transmission lines also appear uniform in 3D space, simulating only a small segment (unit cell) does not account for interaction with

adjacent PWR and GND lines. On the other hand, simulating a power grid structure in entirety of the length is so resource intensive that simulation may not be feasible. To resolve this difficulty we first assume PWR and GND lines are perfectly decoupled and they are at the same RF potential. Thus the interaction between them can be neglected. We later experimentally verify this assumption. With this assumption, both 2D and 3D models are possible which are detailed in the following section.

IV.1 2D Model

The transmission line in power grid schematically shown in Fig 3 can be equivalently represented as cascade of CPW and grounded CPW (CPW-G) transmission line segments. (Fig 4).

Fig 3. Transmission line in power grid is modeled as cascading 2D segments – CPW and CPW-G.

These 2D representations can be solved relatively easy in a 2D EM field solver. Let (Z_1, γ_1) and (Z_2, γ_2) are characteristic impedance and propagation constant of CPW and CPW-G segments respectively (ref. Fig 4).

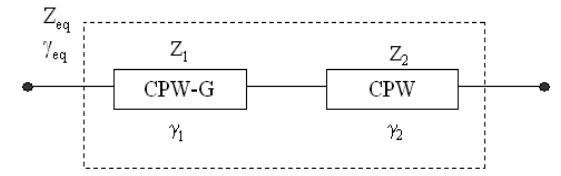

Fig 4. Equivalent line section of the cascaded 2D segments

To find the equivalent characteristic impedance Z_{eq} and γ_{eq} of the cascaded segment we multiply their ABCD matrices as follows,

$$\begin{bmatrix} \cosh\gamma_{eq}l_{eq} & Z_{eq}\sinh\gamma_{eq}l_{eq} \\ Y_{eq}\sinh\gamma_{eq}l_{eq} & \cosh\gamma_{eq}l_{eq} \end{bmatrix} = \begin{bmatrix} \cosh\gamma_1 l_1 & Z_1\sinh\gamma_1 l_1 \\ Y_1\sinh\gamma_1 l_1 & \cosh\gamma_1 l_1 \end{bmatrix} \times \begin{bmatrix} \cosh\gamma_2 l_2 & Z_2\sinh\gamma_2 l_2 \\ Y_2\sinh\gamma_2 l_2 & \cosh\gamma_2 l_2 \end{bmatrix}$$

where l_1 and l_2 are the segment lengths of CPW and CPW-G respectively. l_{eq} is equal to the sum of l_1 and l_2; Y = 1/Z. Under the conditions $\gamma_1 l_1 < 1$ and $\gamma_2 l_2 < 1$(which basically in agreement with eqn. 1), Z_{eq} and γ_{eq} can be written as

$$Z_{eq} = \sqrt{\frac{Z_1\gamma_1 l_1 + Z_2\gamma_2 l_2}{Y_1\gamma_1 l_1 + Y_2\gamma_2 l_2}} \quad (2)$$

$$\gamma_{eq}l_{eq} = \sqrt{\left(Z_1\gamma_1 l_1 + Z_2\gamma_2 l_2\right)\left(Y_1\gamma_1 l_1 + Y_2\gamma_2 l_2\right)} \quad (3)$$

From eqn. 2 and 3, the resistance (R_{eq}) and inductance (L_{eq}) of the cascaded 2D segments are computed as:

$$R_{eq} = r_1 l_1 + r_2 l_2 \quad (4)$$

$$L_{eq} = L_1 l_1 + L_2 l_2 \quad (5)$$

Where (r1, L1) and (r2, L2) are the resistances and inductances per unit length of CPW and CPW-G segments respectively.

From eqn. (4) and (5), it can be inferred that resistive and inductive parameters of the segments can be simply added for the complete response of the equivalent cascaded segments. Further it can also be shown that conductive and capacitive parameters also add up.

IV.2 3D Model

Compared to the 2D models, 3D models can account for the bends and other geometrical variation. Assuming PWR and GND lines are at the same RF potential, we identify different unit cells (fig 5), based on which different transmission line geometries in the grid can be modeled. The unit cells are individually characterized and modeled as 10-port S-parameter box. The models can then be cascaded in a circuit simulator to form the required transmission line geometry. Thus the complexity of computation is substantially reduced as compared to solving the entire structure in a 3D EM field solver.

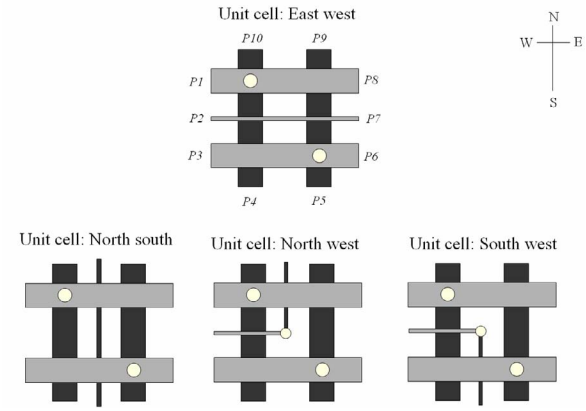

Fig 5. Different unit cell representations of the transmission lines in power grid. These unit cells are modeled as S-parameter black box (10ports) and can be used in circuit simulator.

V Test structures

We validated the proposed modeling methods with a number of power grid transmission line structures. We realized these structures in Wafer Level Packaging (WLP) layers. The WLP is a processing technology that extends the on-chip wiring hierarchy, where wiring layers are fabricated directly (through a post processing step) on top of an active silicon wafer [7]. The distinct advantage of the WLP process

is that it enables a relatively easy fabrication of wide, less resistive yet dense copper lines with thick low-k dielectrics as compared to other processes for on-chip wiring [7]. They are well suited for high quality power distribution and signal transmission.

Fig.6 shows a schematic cross section of the fabricated test chip. It consists of 5 metals of WLP wiring layers post processed on top of a chip representative of 130nm technology. We fabricated two test chips, one with low resistive (20Ω.cm) silicon substrate and other with a high resistive (>4kΩ.cm) silicon substrate to study the substrate influence on transmission line performance.

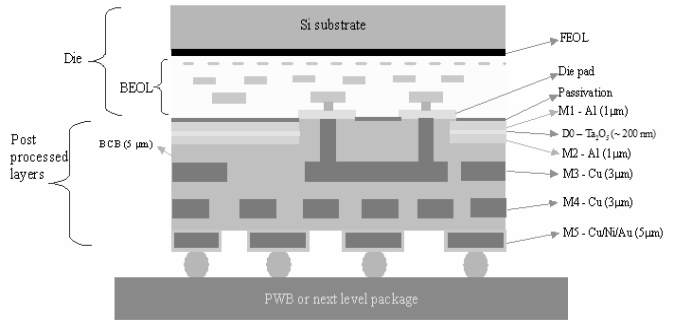

Fig 6. Schematic cross section of the fabricated test chip

The top two WLP layers are realized using 1μm thick aluminum while the next two are 3μm thick copper layers. Bottom most layer (5μm thick Cu/Ni/Au) is used for flip-chip bumping and wire bonding purposes. The aluminum layers are separated by very thin layer of high-k dielectric Ta_2O_5 (ε_r=25), forming capacitor of value 1nF/mm^2 for power supply decoupling applications. Excepting the aluminum layers, other layers are separated by 5μm thick low-k BCB (benzo-cyclobutene, ε_r=2.65) dielectric. The power grids are realized in copper layers. Table1 gives the physical parameters of the fabricated power grid transmission line test structures. Fig 7. shows die photograph of a transmission line test structure in the power grid.

Table 1. Physical parameters of power grid test structures fabricated

Grid size GS (μm)	Signal trace width Ws (μm)	Line lengths L (mm)
25	2.5 to 15 in steps of 2.5	1,5,10,20
50	5 to 30 insteps of 5	1,5,10,20

Note: Width of PWR and GND lines – Wp and Wg are equal to GS

We investigate if the PWR lines in the grid can act as good inherent return path by fabricating three types of power grid structures: Type-A - Power grids with explicitly added decoupling capacitor of value 10nF inserted periodically for every 1mm. This is to ensure PWR and GND lines are nearly at the same RF potential. Type-B - PWR and GND lines are shorted and transmission line structure is now more like CPW. Type-C - Plain grid with no decoupling capacitors or short between PWR and GND.

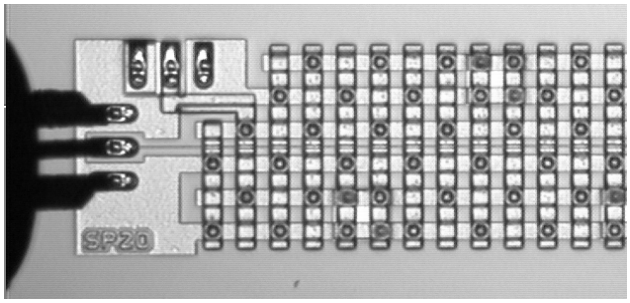

Fig 7. Die photograph of a transmission line test structure in power grid

VI Results and discussion

The test structures were characterized using Vector Network Analyzer (VNA) S-parameter measurement from 45MHz to 50GHz. LRM calibration was used and probe pad parasitics were de-embedded using the method given in [8]. The characteristic impedance and attenuation in dB are extracted for the representative 5μm width, 10mm long transmission line on the 50μm pitch power grid and compared with 2D and 3D models discussed in section IV (Fig 8,9). As can be observed from fig 8,9 the models correlate well with measurements. This correlation confirms our earlier assumption PWR and GND lines in the grid are adequately decoupled and interaction between them can be ignored. Thus grid-modelling requirements are greatly simplified.

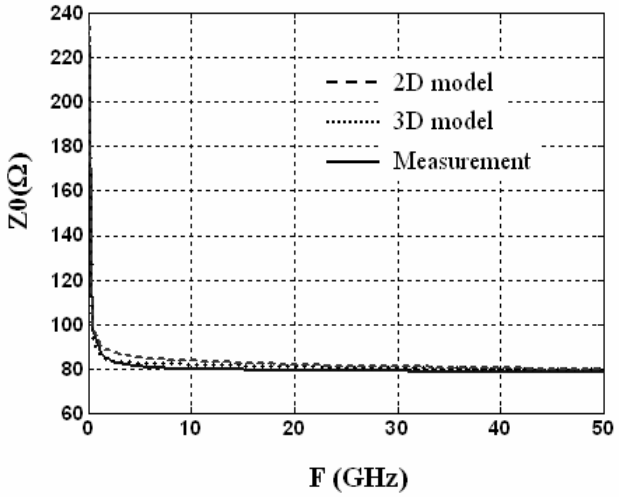

Fig 8. Measured Z0 profile matches well with the models

The correlation also confirms PWR lines act as good return paths as GND lines. One reason could be that the measured transmission line used in the above comparison has decoupling capacitors inserted periodically as explained in the previous section. However it is preferable to have PWR lines inherently act as return path without any periodic decoupling capacitors.

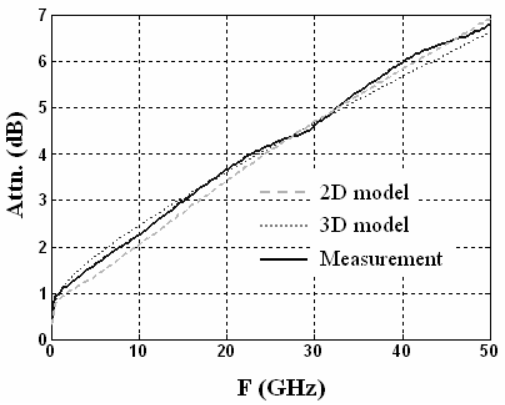

Fig 9. Measured Attenuation profile matches well with models

To test this, we compare measured return (S11) and insertion loss (S12) of three different power grid structures – Type –A, B and C described in the previous section. (Fig 10,11). The return loss and insertion loss completely characterizes the interconnect behaviour. [9].

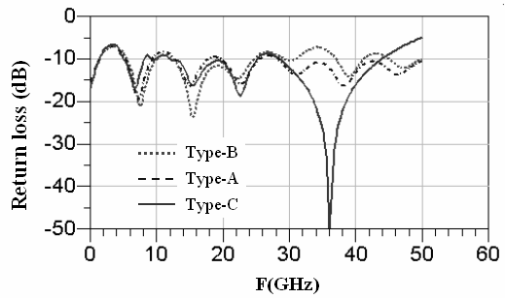

Fig 10. Measured Return loss for the three different grid types

The return loss behaviour is nearly same for all three-grid types up to 30GHz. As can be expected, the insertion loss for the type-B grid (where PWR and GND lines are explicitly shorted) is lowest and is highest for Type-C grid where there is no explicit short or decoupling capacitors. The losses tend to increase sharply beyond 40GHz.

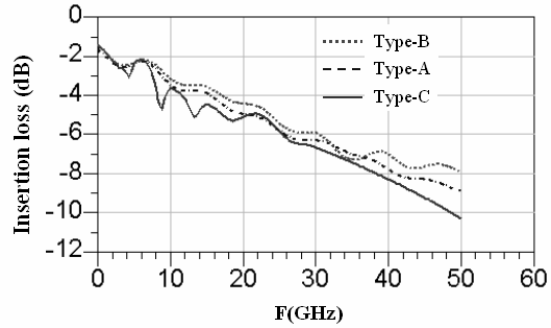

Fig 11. Measured Insertion loss for three different grid types

For frequencies below 30GHz, both insertion and return losses for the three different grid types have marginal difference. However it is not clear how this small difference will affect time domain response. We evaluate the time domain response through eye diagrams. Horizontal and vertical eye openings essentially characterize the quality of signal transmission in time domain. Fig.12 shows the simulated eye response of the transmission lines in the three different grids for 20Gbps PRBS-15 pattern. The measured S-parameters were used to model the transmission lines. The PRBS-15 source has an output impedance of 50Ω and peak-to-peak voltage swing of 350mV. The transmission lines are also terminated with 50Ω.

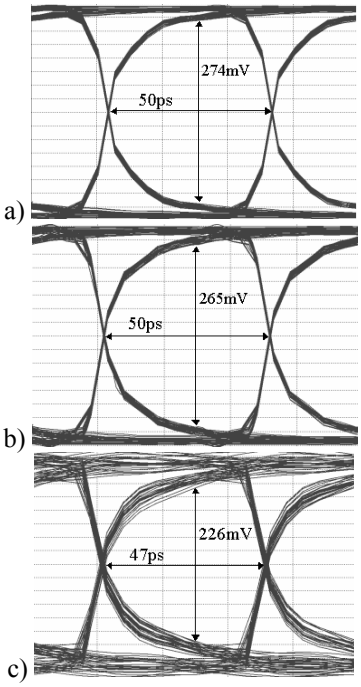

Fig 12. Simulated Eye response of transmission lines in a) Type A, b) Type B and c) Type-C grids.

The eye responses of the type-A and type-B grids are nearly the same whereas rise time of the type-C grid is degraded. The timing jitters on the eye for the three different grids are negligible. However the eye height attenuation (voltage axis) is relatively higher for Type-C grid (3.8ddB) than type-A (2.1dB) and type-B (2.4dB) grids. Further we find difference in eye height attenuation between the type-C and type-A, type-B grids is less than 3dB up to 40Gbps and the timing jitters are negligible. Assuming a 3dB attenuation tolerance, we can approximate the response of the transmission lines in the three different grid types to be nearly the same up to 40Gbps. Thus we conclude the PWR lines inherently act as sufficiently good return path in our design, validating the assumptions made in 2D and 3D models in section IV.

VII. Substrate effects

We find the low resistive silicon substrates influence the performances of power grid transmission lines and they need to be addressed in the design stage. Fig 13 compares

simulated TDT (Time Domain Transmission) response obtained from measured S-parameters of 50 and 25µm pitch power grid transmission lines. The transmission lines in 50µm and 25µm pitch have a width of 5µm and 2.5µm respectively. It can be observed from fig13 in both 50 and 25µm grids, transmission lines in the top metal (Y-layer in fig6) offers lowest delay as compared to bottom layer (X-layer in fig6), although they have same width. Interestingly, delay of the transmission lines in bottom metal layer in 25µm grid is lower than the 50µm grid bottom layer transmission line, despite it's width being double that of 25µm grid transmission line. These effects strongly suggest substrate losses due to substrate conductivity in low resistive substrate. Based on the above observations, design guidelines can be deduced to reduce or mitigate substrate losses. Firstly, the critical signals are to be routed in top most metal layer possible, giving a large separation distance to the substrate. The signals in the bottom layer can be routed in smallest grid pitch possible. Alternatively, slot width – distance between signal and PWR/GND line can be reduced to shield EM fields to the substrate

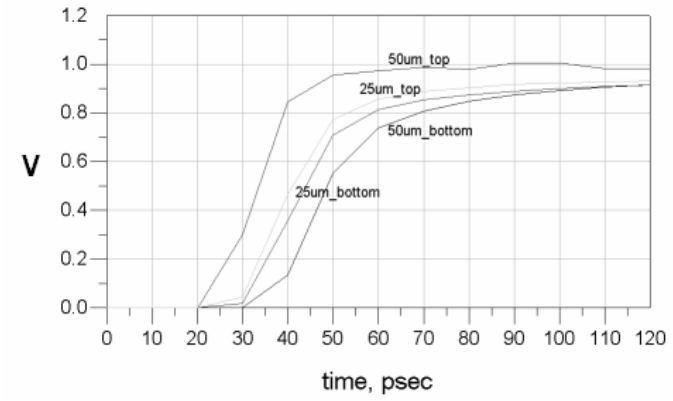

Fig 13. TDT profile for transmission lines in top and bottom layers showing influence of the low resistive silicon substrate

VIII. Conclusion

Transmission lines in power grids simultaneously address power distribution and signal transmission, two of the key issues affecting chip performance in nanometer era. In this paper we analyzed and discussed design oriented modeling methods for laying transmission lines in power grids. We introduced 2D and 3D modelling approaches. In 2D, we modelled the transmission line by cascading CPW and Grounded CPW segments. We also showed mathematically RLGC parameters of the segments add up to form the cumulative total response. We identified different unit cells for 3D modelling. In both 2D and 3D models, modelling complexity was greatly reduced by assuming PWR and GND lines are at the same RF potential and interaction between them can be neglected. We later experimentally validated this assumption through fabricated test structures. We fabricated different power grid test structures in WLP wiring layers and are characterized through S-parameter measurements. The 2D and 3D models correlate well with the measurements. By comparing the measured insertion and return losses as well as with eye response, we showed PWR lines also act as inherent current path as GND lines. Further we analysed substrate effects in the transmission lines on the power grid and found that lower metal layers suffer from substrate losses. These losses manifest as delay in time domain. Based on the observations, we deduced guidelines for designing transmission lines in power grids. These transmission lines can be used for high quality global clock distribution, low latency memory buses and long inter tile interconnections.

Acknowledgements

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