Evaluation of test measures for LNA production testing using a multinormal statistical model

J. Tongbong[1], S. Mir[1] and J.L. Carbonero[2]

[1]TIMA Laboratory
46 Avenue Félix Viallet
38031 Grenoble, France

[2]ST Microelectronics
850 Rue Jean Monnet
38926 Crolles, France

Abstract

For Design-For-Test (DFT) purposes, analogue and mixed-signal testing has to cope with the difficulty of test evaluation before production. This paper aims at evaluating test measures for RF components in order to optimize production test sets and thus reduce test cost. For this, we have first developed a statistical model of the performances and possible test measures of the Circuit Under Test (a Low Noise Amplifier). The statistical multi-normal model is derived from data obtained using Monte-Carlo circuit simulation (five hundred iterations). This statistical model is then used to generate a larger circuit population (one million instances) from which test metrics can be estimated with ppm precision at the design stage, considering just process deviations. With the use of this model, a trade-off between defect level and yield loss resulting from process deviations is used to set test limits. After fixing test limits, we have carried out a fault simulation campaign to verify the suitability of the different test measurements, targeting both catastrophic and single parametric faults. Catastrophic faults are modelled by shorts and opens. A parametric fault is defined as the minimum value of a physical parameter that causes a specification to be violated. Test metrics are then evaluated for the LNA case-study. As a result, test metrics for functional measurements such as S-parameters and Noise Figure are compared with low cost test measurements such as RMS and peak-to-peak current consumption and output voltage, input/output impedance, and the correlation between current consumption and output voltage.

1. Introduction

Production testing of RF components generally targets the validation of the functional specifications. Often, market pressures and reduced testing time limit the number of functional specifications that are actually verified during production. Therefore, following a similar test paradigm as for analogue and mixed-signal components working at low and moderate frequencies, researchers have started to study the optimization of test sets for RF components.

Defect-oriented test techniques have been considered in [3][4][5][6][9]. In [3], industrial results of a quiescent current testing technique are presented. The method is based on varying power supply and observing the corresponding quiescent current signatures. In [4][5], defect testing techniques are presented for non-linear RF front end circuits. In [4] the technique is based on measuring input impedance matching. In [5] they use current consumption as test criteria. In both cases non-intrusive, low cost and low overhead Built-In-Self-Test (BIST) solutions are presented. In [6] a technique using the correlation between current consumption and output voltage of the circuit is used to detect faults, and a low overhead BIST solution implementing this method is proposed. In [9] test measurements include current consumption and only a few more functional tests. But the problem of fixing test limits is not considered. Signature testing based on deriving device specifications from generated signatures is studied in [7]. It is based on reducing test cost by using a low frequency Automated Test Equipment (ATE). Furthermore, in this method, an RF signal modulated by a low frequency signal is injected into the circuit, and then the faults are determined into the demodulated output signal that forms the signature.

Analogue and mixed-signal testing has to cope with the difficulty of test evaluation before production. To evaluate test quality, defect level and yield loss are the major test metrics. In this work, to evaluate and compare test measurements, test limits are fixed following a statistical model of the Circuit Under Test (CUT) and ensuring optimal values of test metrics such as defect level and yield loss in the presence of process deviations at the design stage. The suitability of the test limits is further analyzed by measuring the fault coverage for single catastrophic faults and the test metrics for single parametric faults.

The paper is organized as follows. Section 2 describes the LNA under test. The statistical method used is presented in Section 3. Section 4 will discuss the setting of test limits. In Section 5 fault simulation results are presented. Finally, the paper will conclude with the summary of the obtained results and some directions for future work.

2. LNA description and possible test measures

The CUT is a 0.25 µm BiCMOS cascode 2.2 GHz Low Noise Amplifier (LNA) designed with a ST Microelectronics technology. A similar CUT has been studied in the past in [9]. A schematic description of the LNA is shown in Figure 1. The cascode stage for amplification is surrounded by: biasing stage (resistances R_1-R_{11} and transistors T_1, T_2), decoupling capacitors (C_1, C_3) to dissociate the DC signal (bias signal) of RF signals, coupling capacitors (C_4, C_2), feedback capacitors (C_5, C_6) to protect the cascode stage (transistors T_3, T_2) from a possible over-range voltage and a resistor R_0 added to improve the input adaptation.

978-3-9810801-2-4/DATE07 © 2007 EDAA

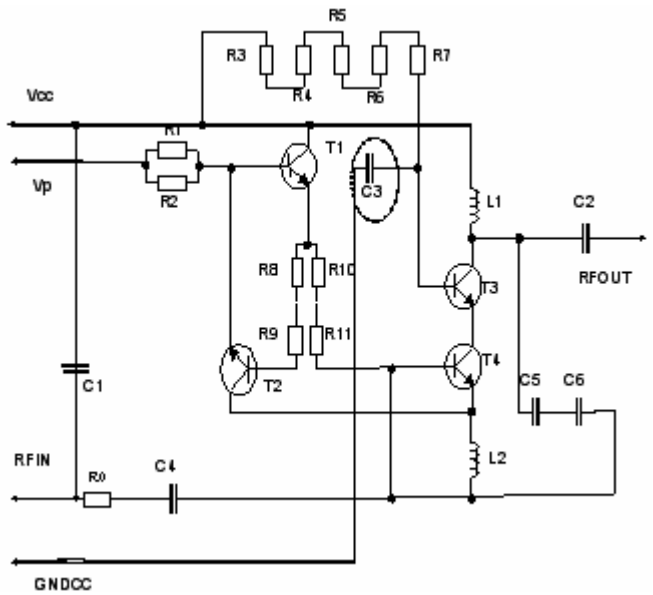


Figure 1. Schematic description of the LNA under test.

On a LNA, the performances typically measured are the gain (S_{21}), Noise Figure (NF), rejection coefficients (S_{11} and S_{22}), compression point (IP_1) and input third order intercept point (IIP_3). In this study we only considered S-parameters and Noise Factor. In addition, we will consider low cost test measurements such as RMS and peak-to-peak current consumption and output voltage, input/output impedance, and the RMS correlation between current consumption and output voltage (I_0). The instantaneous correlation in this case-study is defined as a mathematical function that links total current and output voltage as follows [6]:

$$i0 = \frac{a \cdot i1 + b \cdot i2}{a \cdot b \cdot i1 \cdot i2} \quad (1)$$

where i_1 is the instantaneous current consumption and i_2 is a instantaneous current proportional to the output voltage. Parameters *a* and *b* are fixed as a function of an actual circuit implementation of this correlation function.

In order to find the statistical parameters for the performances and specifications of the CUT, we have performed a Monte Carlo simulation (500 iterations). All physical parameters of all circuit components are varied following their distribution. The statistical parameters of both performances and test measurements are shown in Tables I and II, respectively. Figure 2 shows the distribution of the gain (S_{21}), as an example.

Performances @2.2GHz	**μ**	**σ**
NF (dB)	1.6	0.08
S_{11} (dB)	-12.4	0.46
S_{12} (dB)	-21.9	0.19
S_{21} (dB)	16.3	0.17
S_{22} (dB)	-15.5	1.28

Table I: The performances of the LNA with their statistical parameters: mean value (μ) and standard deviation (σ).

Test measurements	**μ**	**σ**
I_{rms} (mA)	5.2	0.02
I_{pp} (mA)	3.6	0.14
V_{rms} (mV)	44.8	0.89
V_{pp} (mV)	129.3	2.29
I_0 (mA)	15.5	0.05
Z_1 (Ω) @2.2GHz	64.0	1.71
Z_2 (Ω) @2.2GHz	69.1	2.72

Table II: Statistical parameters of possible low cost test measurements.

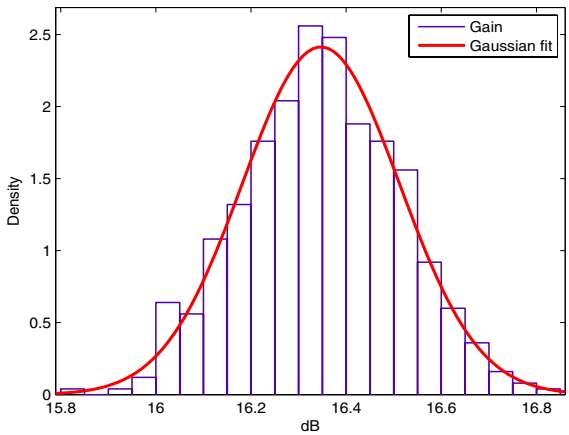


Figure 2. Distribution of the LNA gain.

3. Statistical model: multinormal hypothesis

For measuring analogue test quality, the set of test metrics considered is composed by [1]: Yield Y, Test Yield Y_T, Yield Loss Y_L, Yield Coverage Y_C, and Defect Level D. We will use these metrics in order to set the test limits at the design stage, considering process deviations. Thus we will use the super index D to indicate that the metrics are estimated at the design stage using process deviations. These metrics are:

Y^D=Proportion of functional (good) circuits (2)

Y_T^D=Proportion of circuits that pass the test (3)

Y_L^D=Proportion of functional circuits that fail the test (4)

D^D=Proportion of bad circuits that pass the test (5)

where a functional (or good) circuit is the one for which all its performances are inside their specifications and a bad circuit is the one for which at least one of its specifications is violated.

If A = (A_1, A_2,…, A_n) is the set of the *n* specifications of the performances (A={NF, S_{11}, S_{12}, S_{21}, S_{22}} in our case) and B = (B_1, B_2, …, B_m) the intervals of the accepted values of the *m* test criteria, these metrics are calculated theoretically as follows [2]:

$$Y^D = \int_A fs(s)ds \quad (6)$$

$$Y_T{}^D = \int_B fT(t)dt \quad (7)$$

$$Y_C{}^D = \frac{\int_A \int_B f_{ST}(s,t)dsdt}{Y^D} \quad (8)$$

$$Y_L{}^D = 1 - YC^D \quad (9)$$

$$D^D = 1 - \frac{\int_A \int_B f_{ST}(s,t)dsdt}{Y_T{}^D} \quad (10)$$

where $f_S(s)$ is the joint probability density of the performances; $f_T(t)$ is the joint probability density of the test criteria; and $f_{ST}(s,t)$ is the joint probability density of the performances and the test criteria. Eq (6)-(10) show that test metrics are computed through probability density functions. Under the assumption of a Gaussian distribution function of circuit performances, the density probability functions can be calculated after mathematical operations over the data obtained by a Monte Carlo simulation.

For a p-dimension vector $X= (X_1, X_2, \ldots, X_p)^T$ composed of random variables, with mean value $\mu = (\mu_1, \mu_2, \ldots, \mu_p)^T$ and variance-covariance matrix Σ, if X has a Gaussian distribution, then X has a probability density function (PDF) *f(x)* defined by:

$$f(x) = \frac{1}{\sqrt{\det(2\pi\Sigma)}} \cdot \exp\left[-\frac{(x-\mu)^T \Sigma^{-1}(x-\mu)}{2}\right] \quad (11)$$

This PDF function can then be used to estimate test metrics at the design stage for process deviations using Equations (6)-(10). However, a direct integration of these Equations is normally not feasible when several performances and test measurements are considered. To overcome this problem, we directly use this PDF function to generate by software (MatLab) a population of N=1 million instances that has the same statistical behaviour. From this generated population, the test metrics are estimated as follows:

$$\hat{Y} = \frac{\text{Number of functional circuits}}{N} \quad (12)$$

$$\hat{Y}_T = \frac{\text{Number of circuits that passes the test}}{N} \quad (13)$$

$$\hat{Y}_L = \frac{\text{Number of fail functional circuits}}{\text{Number of functional circuits}} \quad (14)$$

$$\hat{D} = \frac{\text{Number of pass faulty circuits}}{\text{Number of circuits that pass the test}} \quad (15)$$

The assumption of a multinormal hypothesis is verified by plotting the marginal distributions of each performance and test measurement.

4. Setting of test limits

For the case-study LNA, Table III gives the performance limits, which are fixed at 3.9σ of the corresponding mean values. The application of the statistical modeling procedure above defined has resulted in an estimation of 379 circuits being out of specifications due to process deviations.

Performances @2.2GHz	Min	Max
NF (dB)	1.3	1.9
S_{11} (dB)	-14.1	-10.6
S_{12} (dB)	-22.6	-21.1
S_{21} (dB)	15.7	17.0
S_{22} (dB)	-20.5	-10.5

Table III. Specifications limits.

Using the statistical model, we can set test limits as a function of defect level and yield loss under the presence of process deviations. As an example, we will set next the test limits at the point for which defect level and yield loss are equal, thus minimizing both test metrics at the same time. As shown in Figure 3, this point is characterized by 257 *ppm* defect level and test limits of 3.6σ for the RMS current consumption. This means that among the circuit population (1million), 257 of them will be defective due to process deviations. The process deviation fault coverage for RMS current consumption is 32.2% (among the 379 defective circuits, 122 of them are detected). To make a comparison between the possible test measurements, we can use this figure, knowing that each simulation of a normally robust design generates a small number of circuits out of specifications. Table IV gives the test criteria limits fixed at 3.6σ. Figure 4 resumes the different process deviation fault coverage for the potential test criteria.

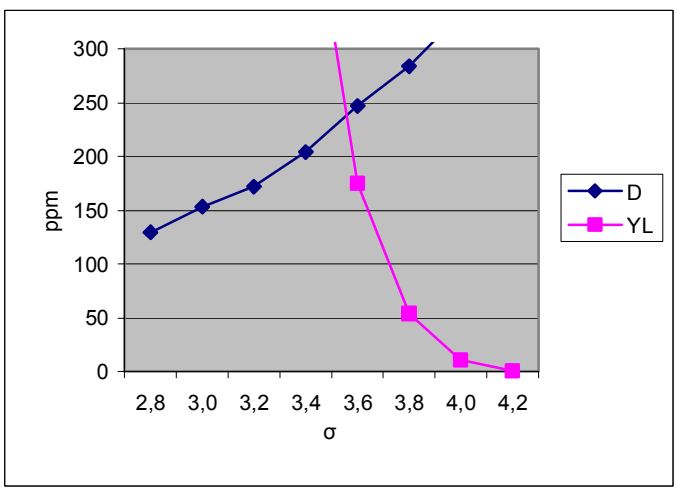


Figure 3. Process deviation Defect level and Yield loss for Irms.

Test measurements	Min	Max
I_{rms} (mA)	5.1	5.3
I_{pp} (mA)	3.1	4.1
V_{rms} (mV)	41.6	48.0
V_{pp} (mV)	121.0	137.6
I_0 (mA)	15.3	15.7
Z_1 (Ω) @2.2GHz	57.9	70.1
Z_2 (Ω) @2.2GHz	59.4	78.8

Table IV. Test measurements limits.

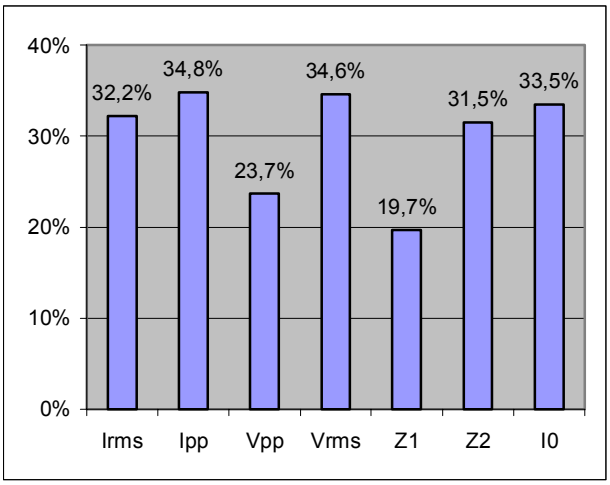


Figure 4. Coverage of faulty behavior due to process deviations at the design stage.

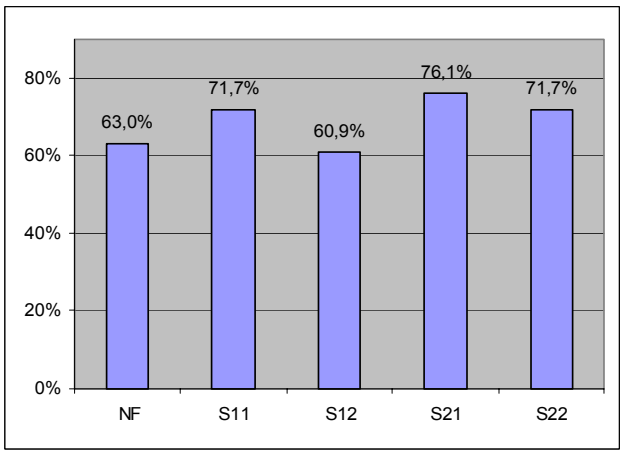
5. Fault simulation results

Once limits for test criteria have been set using the statistical model, and optimizing test metrics for covering process deviations, a fault simulation campaign has been carried out to evaluate these different test metrics in the presence of circuit faults. We have injected both single catastrophic and parametric faults. Multiple faults have not been considered.

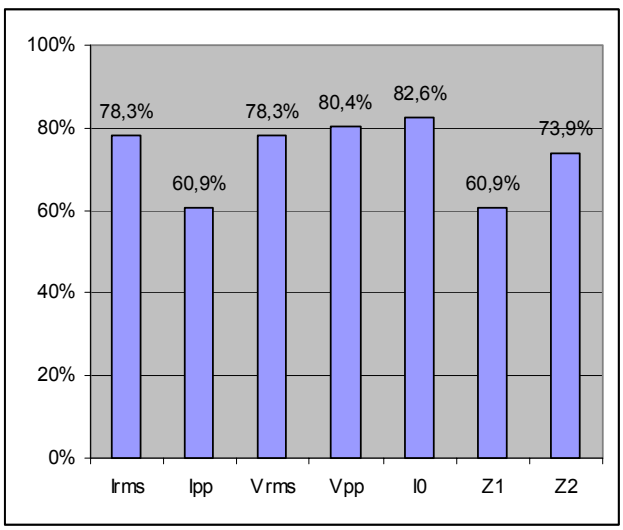
5.1 Catastrophic faults

They result from circuit shorts and opens as it has been done in the past in similar works [9]. Opens have been modeled with a resistance value of 100 MΩ and shorts with a resistor of 1Ω. The faults have been injected in transistors junctions, and also in passive components. Figure 5 shows the fault coverage of each type of test studied for 46 faults.

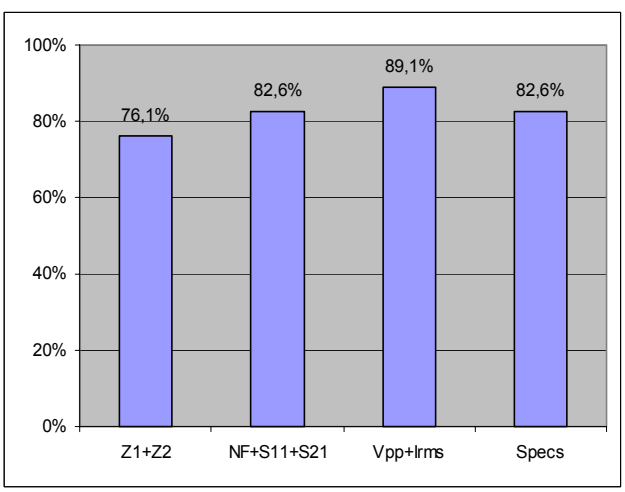
Results on Figure 5 show that the set of specifications can be reduced (with the same fault coverage) to three vectors: NF, S_{11} and gain. These vectors present a fault coverage of 82.6%. Simple test measurements, especially V_{pp} and I_{rms} when added have a higher fault coverage (89.1%) than the set of specifications. The test vector I_0 has a fault coverage of 82.6%, as for the set of all specifications. Faults that are not detected (five in total) are: shorts on the direct junction of transistors in the biasing stage (T_1, T_2), open on decoupling capacitor C_1, and short and open on resistor R_2. For resistor R_2 or R_1, they have been put in parallel to secure the biasing stage, so that a short or an open affecting on one of the two is compensated by the other. An open in this case must be injected on the net before the component. For transistor faults undetected, shorts added on the direct junction do not degrade as much the quality of the junction. These undetected faults result from the setting of the specifications limits.



(a) Specifications fault coverage



(b) Test measures fault coverage



(c) Vector combinations and their fault coverage

Figure 5: Catastrophic fault coverage of different test vectors

5.2 Single parametric faults

5.2.1 Metrics computation

To evaluate the quality of an analogue test with regard to parametric faults, we focus on fault coverage and the test metrics that have been defined in Section 3. These metrics will be calculated following the approach described in [1]. This is illustrated in Figure 6. Given a certain parameter i, a fault is defined as the minimum deviation v_i^{spec} of this parameter that results in the violation of a specification. This probability is noted p_i^{spec} in Figure 6. Similarly, p_i^{test} is defined as the probability that a fault in this parameter is detected by the test, which depends on the minimum deviation v_i^{test} of the parameter that is required for a test criteria to detect the fault.

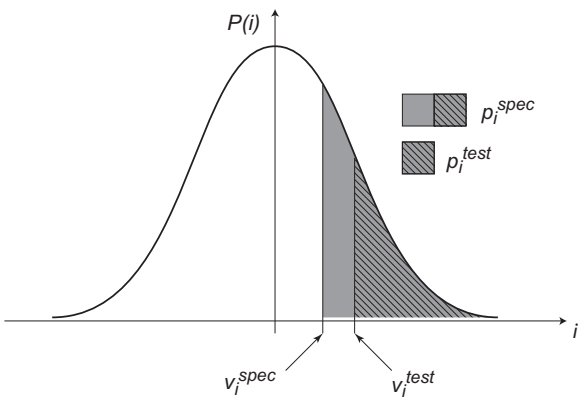


Figure 6. Probability of a parametric fault (p_{spec}) and probability of fault detection (p_{test}) for parameter i.

All the different test metrics can be calculated from these probabilities as shown in [1]. For example, fault coverage is calculated as:

$$F = \frac{\sum_{j=1}^{m} \ln(1 - \min(p_j^{test}, p_i^{spec}))}{\sum_{i=1}^{n} \ln(1 - p_i^{spec})} \qquad (16)$$

where *n* is the number of potential faults and *m* the number of potential faults that can be detected by the test.

5.2.2 Results

The input parameters for simulation consist of 72 local deviations in transistor diffusion length (le) and base width (we), resistance, capacitor and inductances values (C, R, Ls) and passive component width (w). For each of these parameters, we require their standard deviation. It is not possible to obtain these values directly from the Design Kit of the technology. Thus, we have taken example values. For transistor length and width, and passive component width, we have taken a standard deviation of 10 nm. For the values of capacitors, inductances and resistors we have taken a standard deviation of 10% of the nominal value.

A CAT platform developed in the research Group [2] is used to inject the faults described in this parametric fault list. Table V summarizes the collapsed parametric fault list generated for the LNA. The collapsing is done by dropping faults that have very low probabilities (less than 1e-4 in this case) because those faults have a negligible impact on the computation of test metrics.

The test measurements are compared by considering the value of the corresponding test metrics. The test limits of the criteria are the same as those used for the evaluation of catastrophic faults, and they were set using the statistical model from process deviations. The measurement of the input impedance (Z1) shows the best fault coverage (63.5%) and defect level (3.8%). The combination of RMS output voltage and input impedance has the same fault coverage (64.2%) than by considering all the test measurements. As illustrated in Table VI, faults 4 and 5 are never detected by any of the test criteria considered. The high probability of fault n°4 explains why the fault coverage is limited to 64.2%. Table VI resumes the metrics obtained for our test criteria.

We have seen that for catastrophic faults the test set {Vpp, Irms} has the highest fault coverage. This set presents a 60.6% parametric fault coverage. The combination of RMS current consumption and peak to peak output voltage also ensure the best coverage in the case of process deviations. An extended test set {Vpp, Irms, Z_1} will have the same characteristics for catastrophic faults and process deviations, when increasing single parametric faults detection to 64.2%.

We notice also that the yield for process deviations (257 ppm of defective devices for 1 million circuits) is above 99.9 %, while the yield considering parametric faults is just 89.9% (see Table VI). This probably implies that the probabilities of failure obtained in Table V are too high, as a result of standard deviations for the parametric faults being overestimated.

Conclusions

Analogue and mixed-signal testing has to cope with the difficulty of test evaluation before production, and this is especially important for Design-For-Test (DFT) purposes. In this paper, we have illustrated a way to carry out this task and applied it to the case of a LNA case-study. Since the evaluation is done at the design stage, without having production data, test limits are set using a statistical model that considers process deviations. Possible test measurements are then evaluated by considering calculated test metrics. These test metrics can be calculated for the case of process deviations and for the case of single catastrophic and parametric faults. The fault-based approach is used for the selection of the most interesting test criteria. In particular, a test set including peak-to-peak output voltage and RMS current consumption presents good fault coverage for catastrophic and parametric faults.

A test measurement resulting from the correlation between output voltage and current consumption should then be a good test. This is not yet reflected in the results obtained, and we are investigating a better way to compute this correlation. In addition, we are currently extending our parametric fault simulation to cover global parameter variations.

Acknowledgements

We acknowledge the valuable help of Ahcène Bounceur for the use of the CAT platform he has developed. We also acknowledge the feedback of Pr. José Machado in the implementation of the Icc/Vout correlation technique.

Defect N°	Process Parameter (defect)	Deviation	Specification failed	Probabilty of failure
1	Δls (L1)	20.63%	Gain	0.0195
2	Δls (L1)	-18.75%	Gain	0.0303
3	Δls (L2)	8.44%	S22	0.0007
4	Δls (L2)	-5.00%	S22	0.0303
5	Δc (C2)	-16.88%	S11	0.0003
6	Δc (C5)	-24.31%	S12	0.0056
7	Δc (C6)	-25.31%	S12	0.0056
8	Δr (R0)	65.63%	NF	0.0005
9	Δr (R0)	-45.30%	NF	0.0117

Table V: LNA parametric fault list.

Test N°	Test criteria	Defects	F	Y	YT	Yc	D
1	I_{rms}	1, 3, 6	9.2%	89.9%	99.0%	100%	9.2%
2	I_{pp}	None	0%	89.9%	100%	100%	10.0%
3	V_{rms}	1, 3, 6, 8, 9	58.7%	89.9%	92.1%	98.0%	4.3%
4	V_{pp}	1, 3, 6, 8, 9	60.6%	89.9%	88.9%	94.7%	4.1%
5	I_0	3, 6	12.8%	89.9%	98.6%	100%	8.8%
6	Z_1	1, 3, 6, 7, 8, 9	63.5%	89.9%	80.4%	86.0%	3.8%
7	Z_2	1, 3, 6, 7, 8, 9	16.9%	89.9%	94.4%	96.1%	8.4%
8	All test criteria	1, 3 ,6, 7, 8, 9	64.2%	89.9%	77.3%	82.7%	3.7%

Table VI: Test criteria and metrics obtained.

References

[1] S. Sunter, and N. Nagi, "*Test Metrics for Analog Parametric Faults*", Proceedings VTS, 1999, pp. 226-234.

[2] A. Bounceur, S. Mir, L. Rolíndez, and E. Simeu, "*A CAT platform for analogue and mixed-signal test evaluation and optimization*", Digest of Papers of the European Test Symposium, Southampton, UK, 2006, pp. 217-222.

[3] J. Pineda de Gyvez, G. Gronthoud, and R. Amine, "*VDD ramp testing for RF circuits*", IEEE International Test Conference, Charlotte, USA, October 2003, pp. 651-658.

[4] J-Y. Ryu, B.C. Kim, S-T. Kim, and V. Varadarajan, "*Novel defect testing of RF front end using input matching measurement*", In 9th International Mixed-Signal Testing Workshop, Seville, Spain, June 2003, pp. 31-34.

[5] A. Soldo, A. Gopalan, P.R. Mukund, and M. Margala, "*A current sensor for On-Chip, Non-Intrusive Testing of RF Systems*", In Proceedings of the 17th IEEE International Conference on VLSI Design, 2004, pp. 1000-1050.

[6] J. Machado, "*Low-Power In Circuit Testing of a LNA*", In 11th International Mixed-Signal Testing Workshop, Cannes, France, June 2005, pp. 206-210.

[7] R. Voorakaranam, S. Cherubal, and A. Chatterjee, "*A signature test framework for rapid production testing of RF circuits*", In IEEE European Design and Test Conference in Europe, Paris, France, March 2003, pp. 186-191.

[8] N. Nagi, and J. Abraham, "*Hierachical Fault Modeling for analog and mixed-signal circuits*", In IEEE 10th VLSI Test Symposium, Atlantic City, USA, April 1992, pp. 96-101.

[9] R.Kheriji, V.Danelon, J.L Carbonero, S.Mir, "*Optimizing test sets for a Low Noise Amplifier with a defect oriented approach*", DATE, Munich, March 2005,pp. 170-171.

[10] J.T. de Sousa, F. M. Gonçalves, J. P. Teixeira, C. Marzocca, F. Corsi, and T.W. Williams, "*Defect level evaluation in an IC design environment*", In IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 15, N° 10, October 1996, pp. 1286-1293.