Multi-Frequency Wrapper Design and Optimization for Embedded Cores Under Average Power Constraints

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ABSTRACT

This paper presents a new method for designing test wrappers for embedded cores with multiple clock domains. By exploiting the use of multiple shift frequencies, the proposed method improves upon a recent wrapper design method that requires a common shift frequency for the scan elements in the different clock domains. We present an integer linear programming (ILP) model that can be used to minimize the testing time for small problem instances. We also present an efficient heuristic method that is applicable to large problem instances, and which yields the same (optimal) testing time as ILP for small problem instances. Compared to recent work on wrapper design using a single shift frequency, we obtain lower testing times and the reduction in testing time is especially significant under power constraints.

Categories and Subject Descriptors

B.7.2 B.7.3 [**Integrated Circuits**]: [Design Aids, Reliability and Testing]

General Terms

Algorithms, Performance, Design, Reliability

Keywords

Wrapper Design, Multiple Clock Domains, Scan Control Unit

1. INTRODUCTION

Modern systems-on-a-chip (SOCs) use embedded cores that operate internally with multiple clock domains. For example, for a digital video processing SOC reported in [19], the number of clock domains for each core ranges from 2 to 12. In addition, some cores may operate internally at very high rates, typically employing phase-locked loops (PLL) to generate on-chip clocks from far slower external reference signals. For these high performance cores with increasing number of clock domains, there are two major test challenges: (i) Traditional techniques (e.g., I_{DDQ} or functional testing) used for detecting timing-related defects are less effective [7, 13]; (ii) Clock skew during test might corrupt test data and render the test useless [17]. Therefore, to ensure a high quality of defect screening, it is essential that core tests are able to be conducted at rated-speed without clock skew problem.

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Many solutions for scan-based at-speed testing have been introduced [7, 13, 18]. In addition, several techniques [14, 17] have been proposed to test designs with multiple clock domains. However, regardless of their effectiveness, these endeavors mainly consider testing at the chip level and they need to be adapted for testing core-based SOCs, which employ a "divide and conquer" test strategy at core level. On the other hand, most of the existing test wrapper architectures and wrapper design algorithms [2, 5, 6, 9, 11] are only applicable to single-frequency embedded core test. Cumbersome and invasive design techniques such as the insertion of anti-skew latches are needed to make these techniques applicable to current-generation embedded cores. The forthcoming P1500 standard does not provide any direct or non-invasive support for the modular testing of cores with multiple clock domains.

To the best of our knowledge, [21] provides the only strategy in the literature for at-speed testing of cores with multiple clock domains. This solution described a P1500-compliant wrapper [10], which effectively solved the clock skew problem. However its limitation lies in the fact that different clock domains share the same shift clock. Consequently, because this single shift frequency directly impacts the tradeoff between the average power consumption and scan time, excessive test application time (TAT) may result under tight average power constraints. Elevated average power can cause structural damage to the silicon, bonding wires, or the package. It also adds to the thermal load that must be transported away from the core under test. In addition, if all the flip-flops update their state on the same clock edge during shift, the simultaneous switching noise can cause a large voltage drop that may lead to erroneous data transfer, thus invalidating the testing process [12].

The above problems can be addressed by allowing distinct shift frequencies for scan chains in different clock domains, which can be in the range of tens to hundreds of MHz [16, 20] based on the scan chain design and test power requirements. For example, if each clock domain can operate at a distinct shift frequency, lower TAT may be achieved under tight power constraints. Furthermore, by introducing a phase in between the shift clocks used for different clock domains, the number of flip-flops that latch values at the same time will be limited to the number of flip-flops per clock domain, thus avoiding the excessive voltage drop on power/ground lines. Therefore, in this paper, we propose a power-constrained wrapper for cores with multiple clock domains, by extending the design procedure from [21], so that different clock domains can use distinct shift clock signals. Note that these distinct shift clock signals are generated inside the proposed core wrapper. Therefore, unlike in [16], we do not require the tester to shift data at multiple frequencies. Many low- and medium-end testers are not equipped with advanced port scalability features, which allow groups of channels to be driven at different data rates. Thus, the proposed core

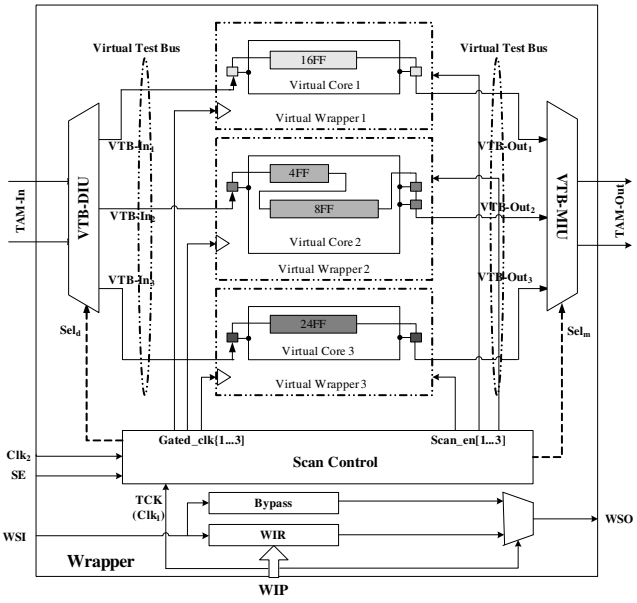


Figure 1: Wrapper Architecture for Multi-Frequency Cores

wrapper allows testing at multiple scan data rates even with less expensive testers. Furthermore, the proposed solution facilitates an added degree of freedom for trading-off power dissipation against scan time, without changing the width of tester lines connected to the core. This will, in turn, enable a better design space exploration of system-level test schedules when both power constraints and the depth of the tester buffers need to be accounted for.

The rest of this paper is organized as follows. Section 2 introduces a novel scan control unit for cores with multiple clocks. Power-constrained wrapper optimization by exploiting multiple shift frequencies is described in Section 3. Experimental results and conclusion are described in Sections 4 and 5 respectively.

2. DESIGN OF SCAN CONTROL UNIT

In this section, we first briefly review the multi-frequency wrapper described in [21], which forms the basis of the proposed solution. Next we discuss the new features of the scan control unit that are required for multiple shift clocks.

In [21], to avoid clock skew during the shift phase in scan testing, logic blocks belonging to different clock domains are grouped as different virtual cores (VCs); see Figure 1. For each VC, a single-frequency virtual wrapper, containing the wrapper scan chains (WSCs) for the respective group, is assigned. At-speed capture for transition-hazard clock domains is controlled by the *scan control* block, which avoids clock skew during the capture phase. In addition, advanced ATPG techniques that are able to handle multi-frequency design as described in [3, 8], are used for test pattern generation. The virtual wrapper is connected to the core interface through internal virtual test bus (VTB) lines. To tradeoff the TAT against test power, the number of internal VTB lines (W_{vtb}) is not necessarily the same as the external test access mechanism (TAM) width assigned to the core (W_{ext}). Instead, the *bandwidth matching*[1] technique [4] is utilized to map the external TAM wires to the internal VTB lines. That is, by introducing frequency converters $VTB-DIU$ ($VTB-MIU$) on the input (output) of the core under test, the internal VTB lines is able to operate at a lower frequency f_s that satisfies $W_{ext} \times f_t \geq W_{vtb} \times f_s$, where f_t is the tester frequency. It is important to note that at-speed test is controlled by on-chip high-speed clock (e.g., from PLL) instead of the tester and, consequently, the proposed technique is particularly relevant when used in conjunction with low-speed testers. To save hardware overhead, both f_s and f_t are determined by dividing f_{TCK} (frequency of TCK, driven by the highest-speed functional clock) by powers of 2. Note that the above is just a brief description of the previously proposed multi-frequency wrapper architecture and, for the sake of completeness, further details can be found in [21].

The scan control block is a major part of the wrapper, which provides the scan enable and shift/capture clock signals to all the VCs. Figure 2(b) depicts the block diagram of the proposed scan control design. When compared to [21] (Figure 2(a)) in which the different VCs share the same shift clock, the proposed clock division unit outputs multiple shift clock signals for different VCs. From the timing diagram shown in Figure 3, we can observe that virtual core 3 is shifted at 50MHz while virtual cores 1 and 2 are shifted at 100MHz. We can also observe that the clock phases of Gated_clock[1] and Gated_clock[2] are different. As a result, the capability to generate distinct shift clocks for different VCs not only expands the solution space during wrapper optimization (as detailed in the following section), but it also decreases the peak power consumption during the scan shift phase. Another novel feature of the proposed scan control unit is that the scan phase is controlled solely on-chip, i.e., it does not need the scan enable signal provided from the automatic test equipment (ATE), as is the case in the previous approach [21]. Since current-generation SOCs may contain tens or even hundreds of cores, if the scan enable signals for all the cores are provided from the ATE, the number of pins available for test data will be reduced, thus increasing TAT [1]. Since the start of the test can be determined by decoding the wrapper instruction and because the length of each test pattern is known, all the scan enable signals can be generated internally. As shown in Figure 2(b), the *TestStart* signal obtained by detecting the change of the wrapper mode to INTEST is used to control the capture finite state machine (FSM) and the mux control unit, which is mainly composed of counters that control the change between the shift and capture phases.

In terms of DFT area, the capture window size and the number of clock domains decide the hardware overhead of the scan control block, which is generally less than 10% of the size of the existing P1500 and scan logic (e.g., when scan and P1500 introduce over 4000 gates, the scan control block adds less than 400 gates [21]). For complex cores with hundreds of thousands of gates this is insignificant, when compared to the benefits of facilitating at-speed multi-frequency test of IP-protected cores.

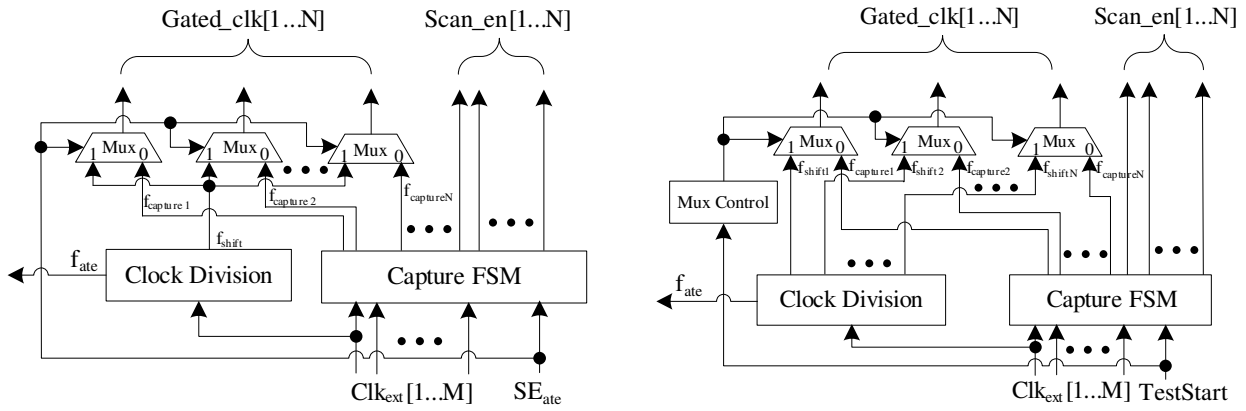
3. WRAPPER OPTIMIZATION

Since the new scan control design enables the scan chains for different clock domains to shift data at distinct frequencies, thereby saving TAT under tight power constraints, we propose a new wrapper optimization procedure to minimize TAT. The problem can be stated as follows:

Problem $P_{mfw-opt}$: Given the test set parameters for the multi-frequency core, including

- the number of clock domains N_C;
- for each clock domain (virtual core) i, the number of primary inputs, primary outputs, and bidirectional I/Os, the number of scan chains and scan chain lengths for fixed-length scan chains (or the number of scan cells when scan chains are flexible); the number of test patterns and the average power consumption P_i;
- the maximum allowed average test power P_{ave};
- the ATE shift frequency f_t;

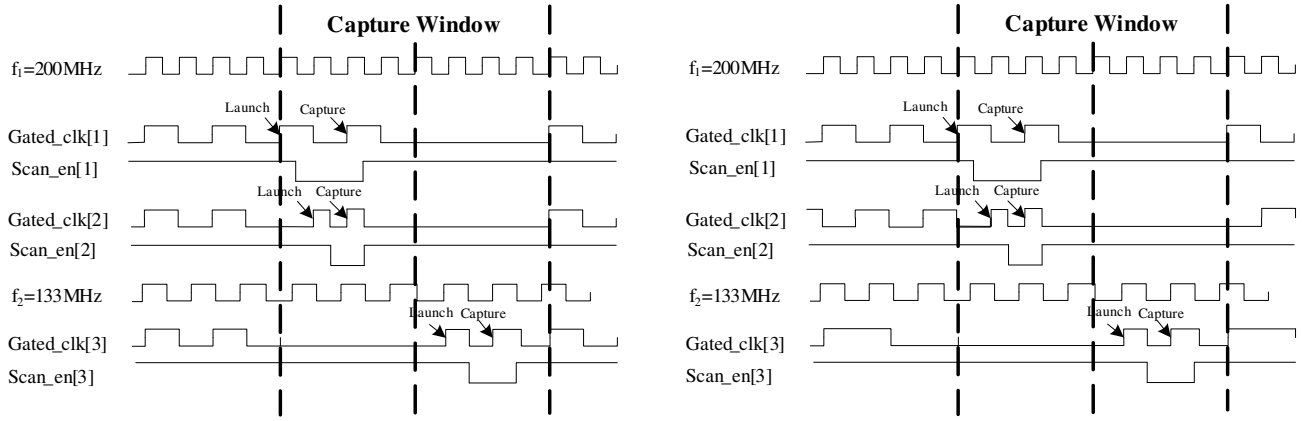
[1] *Bandwidth* is defined as the product of the width and the frequency of a scan architecture.



(a) VCs Share the Same Shift Clock and Scan Enable is Controlled by ATE in [21]

(b) VCs Use Distinct Shift Clocks and Scan Enable is Controlled by On-chip Circuitry

Figure 2: Comparison of Scan Control Blocks



(a) Timing Diagram of the Architecture in [21]

(b) Timing Diagram of the Proposed Architecture

Figure 3: Comparison of Timing Diagrams

- the external TAM width W_{ext};

determine the wrapper design for the core, including

- the shift frequency f_{si} for each clock domain i, $1 \leq i \leq N_C$;
- the number of virtual test bus lines W_i for each clock domain i, $1 \leq i \leq N_C$;
- the wrapper scan chain design

such that the TAT of the core is minimized and the internal scan bandwidth matches the external scan bandwidth.

In this section, we first develop an integer linear programming (ILP) model and solve it using a public software *lp_solve*[2]. Due to the computational cost of the ILP method, we also introduce an efficient heuristic to solve the $P_{mfw-opt}$ problem. Despite its computational complexity, the ILP model is useful to generate optimal solutions for small problem instances, and evaluate the effectiveness of the heuristic method by comparing these exact solutions to the heuristic solutions. The computation time can be reduced by LP-relaxation, whereby some carefully chosen integer variables are allowed to take non-integer values. This results in useful lower bounds on the testing time, which are presented in Section 4.

3.1 Wrapper Optimization using an ILP Model

Suppose the possible shift frequencies for each VC are $f_{si} \in \{F_1, F_2, ..., F_M\}$, which satisfy (i) $F_{k+1} = \frac{F_k}{2}, k \in \{1, 2, ..., M-1\}$ (the "divided by a power of 2" relationship guarantees easy hardware implementation); (ii) $F_1 \times 1 + F_M \times (N_c - 1) \leq f_t \times W_{ext}$, i.e., the external scan bandwidth exceeds the internal bandwidth when the number of VTB lines for every VC is 1 and one clock domain shifts at F_1, while all the other clock domains shift at F_M; and (iii) when all VCs shift at F_M, the maximum allowed average test power P_{ave} is not violated. Hence, when the number of trial frequencies M is given (we assume $M = 4$ in this article), the values of $F_1, ..., F_M$ can be pre-determined based on the above constraints.

Let W_i denote the number of virtual test bus lines assigned to clock domain i. Now the maximum possible value of W_i will be $W_{max} = \frac{f_t}{F_M} \times W_{ext} - N_c + 1$. We are able to pre-calculate $T_i(F_k, j)$, which is the test application time for clock domain i, when W_i is equal to j and f_{si} is equal to F_k. We consider that the given value of P_i is the power consumption for domain i when shifted at F_M. Let us define the binary variable δ_{ij} as $\delta_{ij} = 1$ only if $W_i = j$, where $j \in \{1, 2, ..., W_{max}\}$. In addition, let us define the binary variable θ_{ik} as $\theta_{ik} = 1$ only if domain i is given a shift frequency F_k, where $k \in \{1, 2, ..., M\}$. Then the TAT of the core is:

$$T_{core} = max_i\{\Sigma_{j=1}^{W_{max}} \Sigma_{k=1}^{M} \delta_{ij} \theta_{ik} T_i(F_k, j)\} \quad (1)$$

The following constraints must be satisfied:

1. $\Sigma_{j=1}^{W_{max}} \delta_{ij} = 1$, $1 \leq i \leq N_c$, i.e., every virtual core is assigned to exactly one virtual test bus.
2. $\Sigma_{k=1}^{M} \theta_{ik} = 1$, $1 \leq i \leq N_c$, i.e., every virtual core is shifted in exactly one frequency.

[2]In our experiments we use *lp_solve* from http://elib.zib.de [15].

3. $\sum_{i=1}^{N_c}\sum_{k=1}^{M}\theta_{ik}\times P_i\times\frac{F_k}{F_M}\le P_{ave}$, i.e., the power rating is not exceeded.

4. $\sum_{i=1}^{N_c} W_i\times f_{si}\le W_{ext}\times f_t$, i.e., the external scan bandwidth is not exceeded.

Since we have

$$W_i=\sum_{j=1}^{W_{max}}\delta_{ij}\times j \tag{2}$$

$$f_{si}=\sum_{k=1}^{M}\theta_{ik}F_k=\sum_{k=1}^{M}\theta_{ik}2^{M-k}F_M \tag{3}$$

constraint 4 can be converted to:

$$\sum_{i=1}^{N_c}\sum_{j=1}^{W_{max}}\sum_{k=1}^{M}2^{M-k}\delta_{ij}\theta_{ik}j\le W_{ext}\times(\frac{f_t}{F_M}) \tag{4}$$

The non-linear term $\delta_{ij}\theta_{ik}$, must be linearized so that we can use the linear programming tools to solve this problem. This is done by introducing a new binary variable $\lambda_{ijk}=\delta_{ij}\theta_{ik}$ with additional constraints, which yields the following ILP model:

Objective: Minimize $\max_i\{\sum_{j=1}^{W_{max}}\sum_{k=1}^{M}\lambda_{ijk}T_i(F_k,j)\}$, subject to the following constraints:

1. $\sum_{j=1}^{W_i^{max}}\delta_{ij}=1,\ \ 1\le i\le N_c$
2. $\sum_{k=1}^{M}\theta_{ik}=1,\ \ 1\le i\le N_c$
3. $\sum_{i=1}^{N_c}\sum_{k=1}^{M}2^{M-k}\theta_{ik}P_i\le P_{ave}$
4. $\sum_{i=1}^{N_c}\sum_{j=1}^{W_{max}}\sum_{k=1}^{M}2^{M-k}\lambda_{ijk}j\le W_{ext}\times(\frac{f_t}{F_M})$
5. $\delta_{ij}+\theta_{ik}-\lambda_{ijk}\le 1,\ \ 1\le i\le N_c, 1\le j\le W_{max}, 1\le k\le M$
6. $\delta_{ij}+\theta_{ik}-2\lambda_{ijk}\ge 0,\ \ 1\le i\le N_c, 1\le j\le W_{max}, 1\le k\le M$

It should be noted that with the binary attribute of δ_{ij} and θ_{ik}, the above constraints 5 and 6 effectively constrain $\lambda_{ijk}=\delta_{ij}\theta_{ik}$. The number of variables Num_v and constraints Num_c for this ILP model are $N_cW_{max}+N_cM+N_cMW_{max}$ and $2N_cMW_{max}+2N_c+2$, respectively. Because Num_v and Num_c can easily be in the range of thousands for a core with a large number of N_c and/or W_{ext}, using an ILP solver to obtain the optimal TAM configuration requires large computation time. Hence in the next section we introduce an efficient heuristic for problem $P_{mfw-opt}$, which can achieve near-optimal result within seconds.

3.2 Heuristic for Wrapper Optimization

The algorithm for core wrapper design with multiple shift frequencies (*CWDMSF*) takes as inputs the tester frequency (f_t), the test parameters of the multi-frequency core (C), the TAM width (W_{ext}), the pre-determined possible shift frequency $\{F_1,...,F_M\}$, the number of clock domains N_c and the maximum test power consumption P_{ave}, and it outputs the wrapper design VC, including the shift frequency f_{si} and the number of VTB lines VTB_{VC^i} for each virtual core VC^i. The pseudocode for this procedure is shown in Figure 4.

The algorithm initializes the virtual cores, by assigning to each VC the inputs, the scan chains and the outputs which operate in its clock domain (line 1). In line 2 all the VTB lines are initialized to operate at the lowest possible frequency F_M. Line 3 computes the power consumption P_{curr} (at this moment P_i is the power consumption for clock domain i when shifted at F_M) and if $P_{curr}>P_{ave}$ then

Algorithm 1: *CWDMSF*

INPUT: C, W_{ext}, f_t, N_c, *NoWeights*, $\{F_1,...,F_M\}$, P_{ave}
OUTPUT: f_{si}, $VC=\{VC^i|i=1...N_c\}$

1. Initialize VC;
2. $N_{vtb}=W_{ext}\times\frac{f_t}{F_M}$; $N_{assigned\_vtb}=0$;
3. $P_{curr}=\sum_{i=1}^{N_c}P_i$;
4. **if**($P_{curr}>P_{ave}$) **exit**;
. /*First assign every VC 1-bit VTB line*/
5. **for** i from 1 to N_c {
6. $f_{si}=F_M$; $VTB_{vc^i}=1$;
7. $N_{assigned\_vtb}$++;
8. **do** SFCWD;
. }
. /*Wrapper optimization with different power weight*/
9. **for** *powerWeight* from 0 to $NoWeights-1$ {
10. **while** ($N_{vtb}>N_{assigned\_vtb}$) {
11. find VC^g with TAT $\tau_g=\max\{\tau_i\}$ for all VCs;
12. copy VC^g to VC^{temp};
13. $N_{temp}=N_{assigned\_vtb}$;
14. compute P_{curr};
15. $AssignVTBtoVC(VC^{temp},P_{curr},P_{ave},N_{vtb},N_{temp},powerWeight)$;
16. **if** ($\tau_{temp}<\tau_g$) {
17. copy VC^{temp} to VC^g;
18. $N_{assigned\_vtb}=N_{temp}$;
. } **else** {
19. **break**;
. }
. }
20. $T_{shift}=\max\{\tau_i\}$ for all VCs;
21. record the VC design with the minimum T_{shift};
. }
22. **return** f_{si}, VC;

Figure 4: Pseudocode for Wrapper Design with Multiple Shift Frequencies.

the program exits because it cannot satisfy the power consumption constraint (line 4). Otherwise, each virtual core VC^i is first allocated one VTB line and then a single frequency core wrapper design algorithm *SFCWD* (e.g., *Design_wrapper* [2]) is performed to get an initial testing time (lines 5-8), which will be used as the starting point for virtual test bus line allocation (lines 9-21).

Depending on N_{vtb}, the algorithm proceeds as follows. First, all the virtual cores are sorted based on their TAT and the bottleneck VC (with longest TAT) is identified (line 11). Then the following steps will iteratively assign the remaining VTB lines to virtual cores. The basic idea is to assign more virtual test bus lines to the bottleneck virtual core and at the same time try different possible shift frequencies. Although increasing the frequency will lower TAT, if the current bottleneck VC is assigned a higher frequency without considering the increase in power, a suboptimal solution may be obtained because the available power budget for the next iteration is reduced. To account for this problem, we build a cost function that combines TAT and power, and we select the shift frequency that can obtain the minimum cost instead of minimum TAT. This is done in Algorithm 2 (Figure 5), which assigns VTB lines to the bottleneck VC. *NoWeights* number of power weights in the cost function are tried and we select the one which gives the shortest TAT (line 21).

In Algorithm 2, only one VTB line that operates at F_M is assigned each time. As a result, the bottleneck VC is first transformed to a temporary VC which operates at F_M (line 4). The cost function is built as in line 11, in which *normalWeight* is a constant used to match the TAT and the power consumption into comparable values. In our experiments, we select $NoWeights=100$ and $normalWeight=200$ to limit the run time to a few seconds. Inside the inner loop (lines 8-19), the algorithm selects the shift frequency

Algorithm 2: *AssignVTBtoVC*

INPUT: VC^{temp}, P_{curr}, P_{ave}, N_{temp}, N_{vtb}, *powerWeight*
OUTPUT: τ_{temp}, f_{temp}, $VTB_{VC^{temp}}$, N_{temp}

```
1. τ_orig = τ_temp;
2. P_orig = P_temp; P_others = P_curr − P_orig;
3. while ((τ_temp ≥ τ_orig) && (N_vtb > N_temp)) {
4.     f_temp = F_M; VTB_VC^temp = VTB_VC^temp × f_temp / F_M;
5.     VTB_VC^temp++; N_temp++;
6.     noTrials = M;
7.     minCost = ∞;
.      /*Find the shift frequency with the minimum cost*/
8.     while (−−noTrials > 0) {
9.         do SFCWD;
10.        compute τ_temp, P_temp;
.          /*Build the cost function*/
11.        currCost = (τ_temp − τ_orig)
.                      + powerWeight / normalWeight × (P_temp − P_orig);
12.        if (τ_temp < τ_orig && currCost <= minCost) {
13.            minCost = currCost;
14.            record the current virtual core wrapper design; }
15.        if (VTB_VC^temp %2 == 0 && P_others + 2P_temp <= P_ave) {
16.            f_temp = f_temp × 2;
17.            VTB_VC^temp = VTB_VC^temp ÷ 2;
18.        } else {
19.            break; }
.      }
.  }
20. return τ_temp, f_temp, VTB_VC^temp, N_temp;
```

Figure 5: Procedure for Assigning VTB Lines to the Bottleneck Virtual Core.

that minimize the cost and at the same time satisfies the power constraint (lines 12, 15). Whenever a VTB line is assigned, SFCWD is performed again to get the new testing time (line 9). This program exits when the TAT of the bottleneck VC is reduced or all the virtual test bus lines are assigned with no TAT reduction.

The worst-case complexity of the single frequency wrapper design algorithm *Design_wrapper* is shown to be $O(sc \cdot \log sc + sc \cdot W_{ext})$ in [2], where sc is the number of internal scan chains. The worst-case complexity of the proposed *CWDMSF* algorithm is $O(N_c \cdot \sum_{i=1}^{N_c} sc_i \cdot \log sc_i + W_{ext} \cdot sc_{max} \cdot \log sc_{max} + W_{ext}^2 \cdot sc_{max})$, where sc_i and sc_{max} are the number of internal scan chains for clock domain i and the maximum number of scan chains of all clock domains, respectively. The computational complexity is therefore quadratic in the number of clock domains and the number of external TAM wires. For a core with a fixed number of clock domains, it is quadratic in the number of external TAM wires.

4. EXPERIMENTAL RESULTS

To illustrate the importance of employing multiple shift frequencies in the wrapper architecture, this section shows the comparison between the wrapper design algorithm proposed in this paper and the one based on a single shift frequency reported in [21]. Benchmark SOCs available in the public domain do not contain clock domain information about the embedded cores. Therefore, we present results here for a hypothetical, but representative, multi-frequency embedded core. The hTCADT00 core used in [21] does not have a large number of clock domains and flip-flops. In order to show the TAT variations under power constraints, we have constructed a complex hypothetical multi-frequency core hCADT01. This core has seven clock domains as shown in Table 1, where f_{func} denotes the functional frequency; N_{in}, N_{out}, N_{bi} and N_{sc} are the number of inputs, outputs, bidirectionals and scan chains in the specific clock domain, respectively; the length of each scan chain in clock domain i is shown in column $SC_{length,\ i}$; and P is the power consumption when shifting at 100MHz and is calculated as $P_i = \sum_{j=1}^{|SC_{length,i}|}(l_j | l_j \in SC_{length,i})$. We assume the power consumption of a VC is proportional to the number of memory elements in it. Note that since the maximum internal frequency for the experimental core is $f_{max} = 200MHz$, and we assume that the maximum frequency of the tester is 120MHz in our experiments, the tester will shift test data at $f_t = 100MHz$, thus synchronizing with a division of f_{max}.

Table 2 compares the test application time of hCADT01 when different power constraints P_{ave} are considered. $T_{[21]}$ denotes the TAT for the single frequency shift architecture from [21] and T_{new} stands for the TAT obtained by the multi-frequency shift architecture from this paper derived using the heuristic approach from Section 3.2. ΔT is computed as $\Delta T = \frac{T_{new} - T_{[21]}}{T_{[21]}}$. Even when there is no power constraint (i.e., $P_{ave} = \infty$), we can observe the shifting time is reduced for almost all the given TAM widths from 1 to 16. We can also observe that the proposed architecture leads to much shorter TAT when the power constraint is tighter. For example, when the given TAM width is $W_{ext} \geq 6$ and the power constraint $P_{ave} = 1500$, T_{new} is only half of $T_{[21]}$. This is because all the VCs are constrained to shift at $12.5MHz$ to meet the power requirements in the single-frequency shift architecture from [21], and clock domain 5 ($f_{func} = 50MHz$) dominates with TAT=41.68μs. For the architecture proposed in this paper, clock domain 5 is able to shift at $25MHz$ which results in TAT=20.84μs, while still meeting the power constraint.

We have also implemented the ILP method using a public linear programming solver *lp_solve* [15]. We obtain the same results as the heuristic method when $W_{ext} \leq 4$. When the external TAM width is larger, *lp_solve* does not run to completion in 10 hours, using a 900MHz Pentium III PC with 256MB memory. The execution time of the heuristic is, however, only a few seconds. Nevertheless, the ILP method is useful in that shows the heuristic yields optimal results for $W_{ext} \leq 4$. In addition, for $W_{ext} > 4$, the lower bounds are obtained using LP-relaxation (the variables θ_{ik} and hence also λ_{ijk} in the ILP model were "relaxed" to reals). Due to the nature of LP-relaxation these lower bounds are *not* "tight", which implies that they may *not* be reachable with integer values. The lower bounds for both $W_{ext} \leq 4$ (obtained through ILP) and $W_{ext} > 4$ (from LP-relaxation), are shown in columns T_{lb} of Table 2, from which we can observe that the proposed heuristics generate close values to them.

5. CONCLUSION

We have presented a new method for designing test wrappers for embedded cores with multiple clock domains, by allowing scan chains in different clock domains to shift test data at distinct frequencies. We also proposed an ILP model and efficient heuristics to optimize the wrapper in terms of testing time. Experimental results have been presented for a hypothetical, but representative, multi-frequency embedded core. Compared to recent work on wrapper design using a single shift frequency, we obtain lower testing times, and the reduction is especially significant under power constraints.

6. REFERENCES

[1] S. K. Goel and E. J. Marinissen. Control-Aware Test Architecture Design for Modular SOC Testing. In *Proceedings IEEE European Test Workshop (ETW)*, pages 57–62, Maastricht, The Netherlands, May 2003.

[2] V. Iyengar, K. Chakrabarty, and E. J. Marinissen. Co-Optimization of Test Wrapper and Test Access Architecture for Embedded Cores. *Journal of Electronic Testing: Theory and Applications*, 18(2):213–230, Apr. 2002.

$f_{func}(MHz)$	N_{in}	N_{out}	N_{bi}	P	N_{sc}	$SC_{length,\ i}$
200	109	32	72	2572	16	{168 168 166 166 163 163 163 163 162 162 162 162 151 151 151 151}
133	144	67	72	450	3	{150 150 150}
120	89	8	72	930	10	{93 93 93 93 93 93 93 93 93 93}
75	111	31	72	1314	6	{219 219 219 219 219 219}
50	117	224	72	2605	5	{521 521 521 521 521}
33	146	68	72	576	11	{82 82 82 81 81 81 18 18 17 17 17}
25	15	30	72	40	4	{10 10 10 10}

Table 1: hCADT01 Clock Domain Information

	$P_{ave} = 1500$				$P_{ave} = 3000$				$P_{ave} = 4500$				$P_{ave} = \infty$			
W_{ext}	T_{lb}	$T_{[21]}$	T_{new}	$\Delta T(\%)$	T_{lb}	$T_{[21]}$	T_{new}	$\Delta T(\%)$	T_{lb}	$T_{[21]}$	T_{new}	$\Delta T(\%)$	T_{lb}	$T_{[21]}$	T_{new}	$\Delta T(\%)$
16	20.84	41.68	20.84	-50	10.42	20.84	10.42	-50	6.72	10.42	7.44	-28.60	6.4	7.94	7.44	-6.30
15	20.84	41.68	20.84	-50	10.42	20.84	10.42	-50	6.91	10.42	8.76	-15.93	6.8	9.59	7.49	-21.90
14	20.84	41.68	20.84	-50	10.42	20.84	10.42	-50	7.51	10.42	8.88	-14.80	7.33	10.42	8.88	-14.78
13	20.84	41.68	20.84	-50	10.42	20.84	10.42	-50	8.17	10.42	10.42	0	7.99	10.42	9.59	-7.97
12	20.84	41.68	20.84	-50	10.42	20.84	10.42	-50	8.79	10.42	10.42	0	8.73	10.42	10.42	0
11	20.84	41.68	20.84	-50	10.42	20.84	11.62	-44.24	9.62	10.92	10.42	-4.58	9.44	10.92	10.42	-4.58
10	20.84	41.68	20.84	-50	10.51	20.84	12.08	-42.03	10.42	12.78	11.62	-9.08	10.33	12.78	11.62	-9.08
9	20.84	41.68	20.84	-50	11.51	20.84	13	-37.62	11.33	13.78	12.78	-7.26	11.33	13.78	12.78	-7.26
8	20.84	41.68	20.84	-50	12.93	20.84	14.48	-30.52	12.82	15.88	14.88	-6.30	12.81	15.88	14.88	-6.30
7	20.84	41.68	20.84	-50	14.73	20.84	17.76	-14.78	14.73	20.84	15.63	-25	14.73	20.84	15.63	-25
6	20.84	41.68	20.84	-50	17.52	20.84	20.84	0	17.52	20.84	19.2	-7.87	17.52	20.84	19.18	-7.97
5	21.24	41.68	25.04	-39.92	20.85	25.56	23.24	-9.08	20.85	25.56	23.24	-9.08	20.85	25.56	23.24	-9.08
4	29.76	41.68	29.76	-28.60	29.76	31.76	29.76	-6.30	29.01	31.76	29.01	-8.66	29.01	31.76	29.01	-8.66
3	41.68	41.68	41.68	0	38.36	41.68	38.36	-7.97	38.36	41.68	38.36	-7.97	38.36	41.68	38.36	-7.97
2	59.88	63.52	59.88	-5.73	58.02	63.52	58.02	-8.66	58.02	63.52	58.02	-8.66	58.02	63.52	58.02	-8.66
1	116.04	127.04	116.04	-8.66	116.04	127.04	116.04	-8.66	116.04	127.04	116.04	-8.66	116.04	127.04	116.04	-8.66

Table 2: Comparison of Test Application Time for hCADT01 with Different Power Constraints

[3] V. Jain and J. Waicukauski. Scan Test Data Volume Reduction in Multi-clocked Designs with Safe Capture Technique. In *Proceedings IEEE International Test Conference (ITC)*, pages 148 –153, Oct. 2002.

[4] A. Khoche. Test Resource Partitioning for Scan Architectures Using Bandwidth Matching. In *Digest of Int. Workshop on Test Resource Partitioning*, pages 1.4.1–1.4.8, 2002.

[5] S. Koranne. A Novel Reconfigurable Wrapper for Testing of Embedded Core-Based SOCs and its Associated Scheduling Algorithm. *Journal of Electronic Testing: Theory and Applications*, 18(4/5):415–434, Aug. 2002.

[6] E. Larsson and Z. Peng. A Reconfigurable Power-Conscious Core Wrapper and its Application to SOC Test Scheduling. In *Proceedings IEEE International Test Conference (ITC)*, pages 1135–1144, Charlotte, NC, Sept. 2003.

[7] X. Lin, R. Press, J. Rajski, P. Reuter, T. Rinderknecht, B. Swanson, and N. Tamarapalli. High-Frequency, At-Speed Scan Testing. *IEEE Design & Test of Computers*, 20(5):17–25, Oct 2003.

[8] X. Lin and R. Thompson. Test generation for designs with multiple clocks. In *Proceedings ACM/IEEE Design Automation Conference (DAC)*, pages 662 –667, 2003.

[9] E. J. Marinissen et al. A Structured And Scalable Mechanism for Test Access to Embedded Reusable Cores. In *Proceedings IEEE International Test Conference (ITC)*, pages 284–293, Washington, DC, Oct. 1998.

[10] E. J. Marinissen et al. On IEEE P1500's Standard for Embedded Core Test. *Journal of Electronic Testing: Theory and Applications*, 18(4/5):365–383, Aug. 2002.

[11] E. J. Marinissen, S. K. Goel, and M. Lousberg. Wrapper Design for Embedded Core Test. In *Proceedings IEEE International Test Conference (ITC)*, pages 911–920, Atlantic City, NJ, Oct. 2000.

[12] N. Nicolici and B. M. Al-Hashimi. *Power-Constrained Testing of VLSI Circuits*. Kluwer Academic Publishers, 2003.

[13] S. Pateras. Achieving At-Speed Stuctural Test. *IEEE Design & Test of Computers*, 20(5):26–33, Oct 2003.

[14] J. Schmid and J. Knablein. Advanced Synchronous Scan Test Methodology for Multi Clock Domain ASICs. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 106 – 113, 1999.

[15] H. Schwab. Lp solve. In *http://elib.zib.de/pub/Packages/mathprog/linprog/lp-solve*, 1997.

[16] A. Sehgal and K. Chakrabarty. Efficient Modular Testing of SOCs Using Dual-Speed TAM Architectures. In *Proceedings Design, Automation, and Test in Europe (DATE)*, pages 422–427, Paris, France, Feb. 2004.

[17] Technical White Paper. Designs with Multiple Clock Domains: Avoiding Clock Skew and Reducing Pattern Count Using DFT Advisor and Fast Scan. http://www.mentor.com/dft.

[18] N. Tendolkar, R. Raina, R. Woltenberg, X. Lin, B. Swanson, and G. Aldrich. Novel Techniques for Achieving High At-Speed Transition Fault Test Coverage for Motorola Microprocessors Based on PowerPC Instruction Set Architecture. In *Proceedings IEEE VLSI Test Symposium (VTS)*, pages 3–8, 2002.

[19] B. Vermeulen, S. Oostdijk, and F. Bouwman. Test and Debug Strategy of the PNX8525 Nexperia^{TM} Digital Video Platform System Chip. In *Proceedings IEEE International Test Conference (ITC)*, pages 121–130, Oct. 2001.

[20] D. Wu, M. Lin, S. Mitra, K. S. Kim, A. Sabbavarapu, T. Jaber, P. Johnson, D. March, and G. Parrish. H-DFT: A Hybrid DFT Architecture for Low-Cost High Quality Structural Testing. In *Proceedings IEEE International Test Conference (ITC)*, pages 1229 – 1238, 2003.

[21] Q. Xu and N. Nicolici. Wrapper Design for Testing IP Cores with Multiple Clock Domains. In *Proceedings Design, Automation, and Test in Europe (DATE)*, pages 416–421, Paris, France, Feb. 2004.