Self-Biased High-Bandwidth Low-Jitter 1-to-4096 Multiplier Clock Generator PLL

John G. Maneatis[1], Jaeha Kim[1], Iain McClatchie[1], Jay Maxey[2], Manjusha Shankaradas[2]

[1]True Circuits, Inc.
4962 El Camino Real, Suite 206
Los Altos, CA 94022
(650) 691-7601
maneatis@truecircuits.com

[2]Texas Instruments Incorporated
12500 TI Boulevard, MS 8664
Dallas, TX 75243
(214) 480-4472
j-maxey@ti.com

ABSTRACT

A self-biased PLL uses a sampled feed-forward filter network and a multi-stage inverse-linear programmable current mirror for constant loop dynamics that scale with reference frequency and are independent of multiplication factor, output frequency, and PVT. The PLL achieves a multiplication range of 1 to 4096 with less than 1.7% output jitter. Fabricated in 0.13µm CMOS, the area is 0.182mm^2 and the supply is 1.5V.

Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Types and Design Styles - *input/output circuits, VLSI*.
B.4.3 [**Input/Output and Data Communications**]: Interconnections - *asynchronous/synchronous operation, interfaces*.
B.8.m [**Performance and Reliability**]: Miscellaneous.

General Terms: Algorithms, Design, Performance, Reliability.

Keywords: Phase-locked loop, PLL, frequency synthesis, clock generation, clock multiplication, self biased, adaptive bandwidth, analog circuits.

One challenge in designing phase-locked loops (PLLs) for ASICs is providing ample flexibility for a wide variety of applications, including processors and video/chip interfaces. Satisfying diverse clock generation applications with a single PLL design requires that it be capable of multiplying by a wide range of factors while operating with a high bandwidth that tracks the reference frequency. This requirement is important to minimize the tracking/long-term jitter without sacrificing the period/short-term jitter performance, to operate over a wide output frequency range, and to offer optimal performance at any operating condition without being compromised by its generality. This paper describes a self-biased clock generator PLL capable of multiplying by 1 to 4096 with near constant period jitter over the whole range. The PLL extends the self-biased PLL architecture [1] with a new loop filter structure that produces constant loop dynamics that scale with reference frequency and are virtually independent of the multiplication factor, output frequency, process, and environmental conditions.

A key problem facing any clock generator PLL design is the period jitter that repeats in a pattern every N output cycles, where N is the PLL multiplication factor. This pattern jitter is due to the charge pump, which transfers charge for only a short period of time and develops a short proportional control signal that affects the N output cycles unequally. A common remedy is to add a shunt capacitor to the series RC network that spreads the charge over a longer period, desirably over N or more output cycles, and develops less signal amplitude. However, the extended charge transfer period is fixed in number of output cycles for a given shunt capacitance and output frequency, which becomes problematic when N needs to vary over a wide range. With a high loop bandwidth, transfer periods longer than N cycles degrade PLL stability while shorter transfer periods cause pattern jitter. To accommodate a wide range of multiplication factors N, the charge transfer period must scale linearly with N.

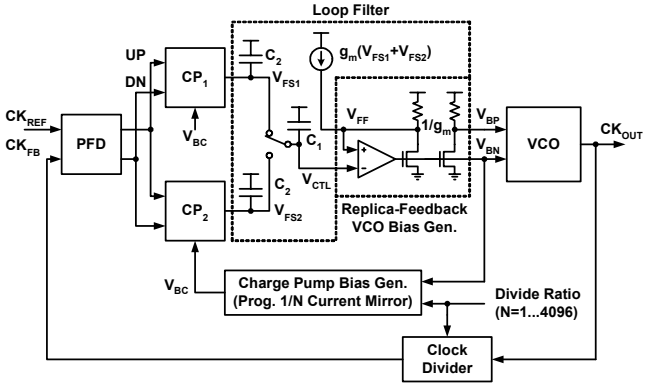

Figure 1: Self-biased clock generator PLL architecture.

The block diagram of the self-biased clock generator PLL is shown in Figure 1. It uses a sampled feed-forward network to spread the charge uniformly over the reference cycle, or N output cycles, as desired. Unlike the circuits used in related techniques reported [2], this network is simple in structure and lends itself well to self-biased techniques. The network produces both the proportional (V_{FF}) and integral (V_{CTL}) control signals needed to properly stabilize the PLL. The network consists of two transfer

DAC 2003, June 2-6, 2003, Anaheim, California, USA.

paths that alternate every comparison cycle. For each cycle, one of the two identical charge pumps dumps the error charge onto its output capacitor C_2, which develops a voltage V_{FS1} (V_{FS2}) that remains constant for the duration of the cycle. In the meantime, the other output capacitor is shorted to the capacitor C_1 at V_{CTL} to convert this proportional signal into an integral signal of smaller magnitude (C_2/C_1). Using the transconductance (g_m) stage, the two voltages are summed and driven as a current into a matching $1/g_m$ resistance inside the bias generator where, as the proportional signal, they are summed with V_{CTL}. Two C_2 capacitors are used to allow a whole comparison cycle for charge equalization. More filtering can be obtained by using m+1 C_2 capacitors where each is active for m cycles with a gain of 1/m. Also, the network can be further simplified by splitting the negative input of the amplifier to sum V_{FS1} and V_{FS2} directly without connecting to V_{CTL}.

Extending the analysis in [1] for the proposed filter network will show that the bandwidth to reference frequency ratio and the damping factor are given by the equations

$$\frac{\omega_N}{\omega_{REF}} = \frac{1}{\omega_{REF}} \cdot \sqrt{\frac{1}{N} \cdot I_{CH} \cdot K_V \cdot \frac{1}{C_1}} = \frac{\sqrt{x \cdot N}}{2\pi} \cdot \sqrt{\frac{C_B}{C_1}}$$

$$\zeta = \frac{1}{2} \cdot \omega_N \cdot R \cdot C_1 = \frac{\sqrt{x \cdot N}}{4} \cdot \frac{\sqrt{C_B \cdot C_1}}{C_2}$$

where x is the set ratio of the charge pump current to the VCO bias current (I_{CH}/I_B) and C_B is the effective VCO capacitance such that $F_{VCO}=g_m/C_B$. These equations suggest that if the ratio I_{CH}/I_B is set to 1/N, the PLL will have constant loop dynamics independent of multiplication factor, output frequency, process, and environmental conditions.

Generating a charge pump current that is 1/N of the VCO bias current can be done by adjusting the size ratio of a current mirror. However, simply segmenting the diode-connected side will require excessively large devices to realize ratios as large as 4096:1. Instead, as shown in Figure 2, this PLL uses a multi-stage programmable current source as the diode-connected side of the mirror. This current source is composed of 4 binary-weighted

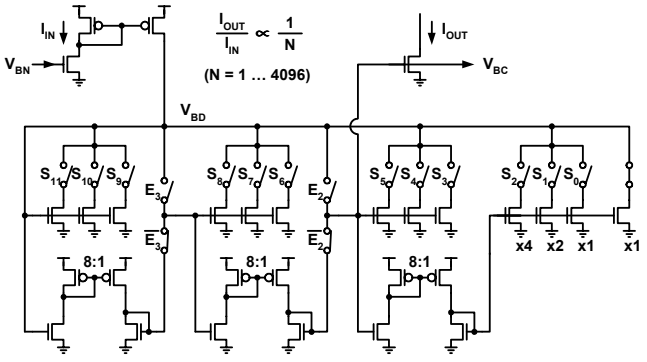

Figure 2: Inverse-linear programmable current mirror.

groups, each covering a range of 0-7 and separated by 8:1 gain reducing stages. As such, the mirror will divide the input current by N, where N ranges from 1 to 4096. The output bias V_{BC} can be tapped from any of the gain reducing stages for fixed current scaling. For small N, the extra switches E_2 and E_3 bypass the unused more significant stages to avoid large voltages at the diode connection point V_{BD}. To ensure stability, the gain-reducing stages must have gain less than one.

This self-biased clock generator technique can be applied to most VCO circuit families. In this PLL, the VCO circuits, shown in Figure 3, are similar to those previously published [1]. The VCO

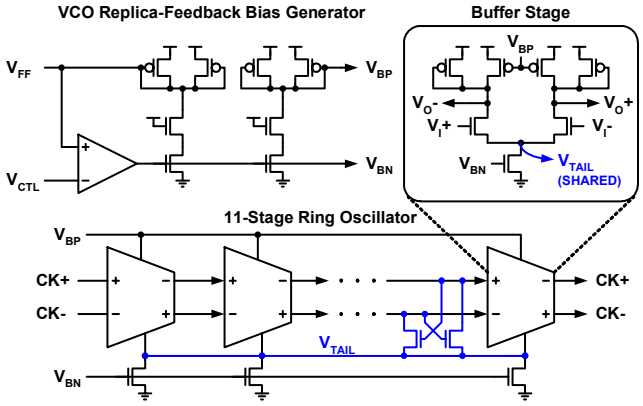

Figure 3: Voltage-controlled oscillator circuits.

is a ring oscillator composed of symmetric-load buffer stages with replica feedback biasing for high supply noise rejection. To further improve the supply noise rejection, the center nodes V_{TAIL} of the differential pairs are shorted together in order to make the voltages more closely match the corresponding voltage inside the half-buffer replica despite the nonlinear output resistance of the current sources. However, this short converts the differential ring into two single-ended rings. To ensure differential operation, the input transistors of one stage pair are split and cross-connected to the stage outputs. Other cross-coupling points can be used to marginally increase or decrease the oscillation frequency. The matching loop filter circuits, shown in Figure 4, use half-buffer replicas as the transconductance stage matching the $1/g_m$-resistance in the bias generator. The select block enables the charge pump just before the beginning of the comparison cycle in order to maximize the period that V_{FS1} (V_{FS2}) stays constant.

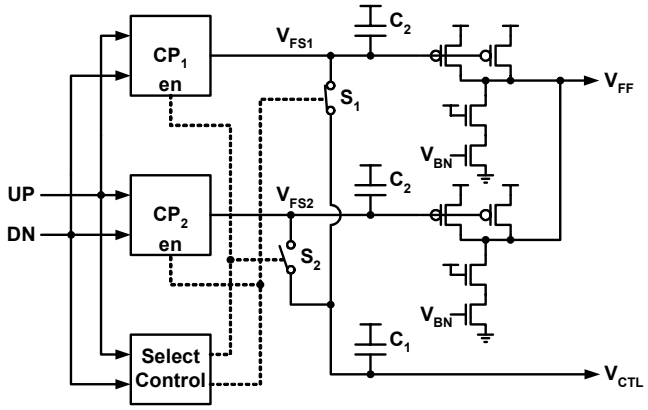

Figure 4: Sampled feed-forward filter network.

The clock generator PLL was fabricated in a 0.13µm N-well CMOS process. A micrograph of the fabricated PLL is shown in Figure 5 and the performance characteristics of the PLL are summarized in Figure 6. Figure 7 is a plot of the measured tracking jitter and period jitter as a function of N for a fixed output frequency of 240MHz. The tracking jitter increases linearly with N because the bandwidth decreases. However, the period jitter is relatively constant with N, ranging from 1 to 4096, demonstrating the effectiveness of the sampled feed-forward network.

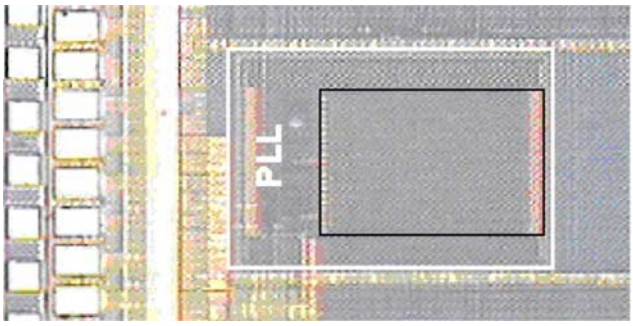

Figure 5: Die micrograph of self-biased clock generator PLL.

Process Technology	0.13µm nwell CMOS
Nominal Supply Voltage	1.5V
Total Occupied Area	0.38 x 0.48 mm^2
VCO Frequency Range	30 ~ 650 MHz
Multiplication Factor Range	N = 1 ~ 4096
Power Dissipation	7 mW @ 240 MHz, 1.5V
Period Jitter (quiescent)	30.5 ps (p-p), 4.0 ps (rms) @ N = 1
@ 240 MHz Output	37.2 ps (p-p), 4.2 ps (rms) @ N = 1024
	42.7 ps (p-p), 4.3 ps (rms) @ N = 4096
	72.6 ps (p-p), 18.8 ps (rms) @ worst-case
Period Jitter (noise*)	44.6 ps (p-p), 4.9 ps (rms) @ N = 1024
Tracking Jitter (quiescent)	43.9 ps (p-p), 4.6 ps (rms) @ N = 1
@ 240 MHz Output	7.47 ns (p-p), 939 ps (rms) @ N = 1024
Tracking Jitter (noise*)	7.62 ns (p-p), 1.07 ns (rms) @ N = 1024
Reference Sidebands	-35 dBc @ N = 1024, 240 MHz Out

* At 240MHz output with 100mV of 100kHz square wave supply noise

Figure 6: PLL performance summary.

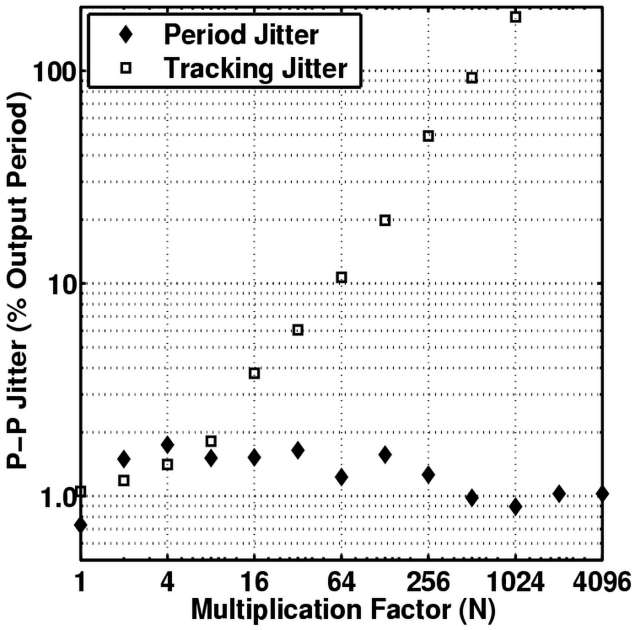

Figure 7: Jitter versus multiplication factor at fixed 240MHz output.

REFERENCES

[1] J. Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques," *IEEE J. Solid-State Circuits*, vol. 31, no. 11, pp. 1723-1732, Nov. 1996.

[2] A. Maxim, et al., "A Low-Jitter 125-1250 MHz Process-Independent 0.18µm CMOS PLL Based on a Sample-Reset Loop Filter," *ISSCC 2001 Dig. Tech. Papers*, pp. 394-395, Feb. 2001.