Single-Phase Source-Coupled Adiabatic Logic

Suhwan Kim and Marios C. Papaefthymiou

Advanced Computer Architecture Laboratory
Department of Electrical Engineering and Computer Science
University of Michigan
Ann Arbor, MI 48109

Abstract

Adiabatic circuits offer a promising alternative to conventional circuitry for low energy design. Their operation is nevertheless subject to fundamental energy-speed trade-offs, just like any other physical realization of boolean logic. Thus, adiabatic circuits with very low energy consumption at low frequencies fail to function at high operating frequencies. Conversely, high-speed adiabatic circuits tend to be dissipative at low clock rates.

This paper describes SCAL, a single-phase source-coupled adiabatic logic family that operates efficiently across a wide range of operating frequencies. In layout-based simulations with 0.5μm CMOS process parameters, pipelined carry-lookahead adders developed in our logic function correctly from 10MHz up to 280MHz. Our SCAL adders are less dissipative than corresponding designs in alternative adiabatic families that remain functional across the same frequency range. Moreover, they are about as dissipative as other adiabatic circuits that are geared towards very efficient operation at low frequencies. In comparison with their CMOS counterparts, our SCAL adders are 3 to 10 times more energy efficient.

1 Introduction

Adiabatic circuit architectures reduce energy dissipation by steering currents across devices with low voltage differences and by recycling the energy stored in their capacitors [2, 3]. Broadly speaking, the efficient operation of these designs is yet another manifestation of energy-speed trade offs. Consequently, adiabatic circuits that operate very efficiently at low operating frequencies stop functioning at high data rates. On the other hand, adiabatic circuits with broad operating ranges tend to be dissipative at low frequencies.

This paper presents a source-coupled adiabatic logic family, called SCAL, that achieves very low dissipation across a wide range of operating frequencies. High speed is ensured by activating a sense-amplifier structure in a nonadiabatic manner. High energy efficiency across a broad frequency range is achieved by providing each gate with a current source that can be tuned by transistor sizing to achieve optimal charging rates for its operating conditions. In addition to low energy consumption and broad operating spectrum, SCAL features include true single-phase operation, balanced clock loading, functional completeness, and straightforward cascading.

A plethora of adiabatic logic families has been proposed in recent years. Several of these families, including 2N-2P, 2N-2N2P, PAL, CAL, and TSEL, use a sense-amplifier structure to drive their outputs adiabatically [4, 6, 7, 8, 9]. The logic family we present in this paper is an enhancement of TSEL, a true single-phase adiabatic logic. SCAL achieves increased energy efficiency across a broad frequency range while at the same time maintaining all the positive aspects of TSEL.

The remainder of this paper has four sections. The structure and operation of our logic is described in Section 2. Section 3 describes the operation of cascaded SCAL gates. Section 4 presents simulation results from layouts of pipelined 4-bit CLAs that were designed using a 0.5μm standard CMOS technology. Our contributions and ongoing research are summarized in Section 5.

2 SCAL Structure and Operation

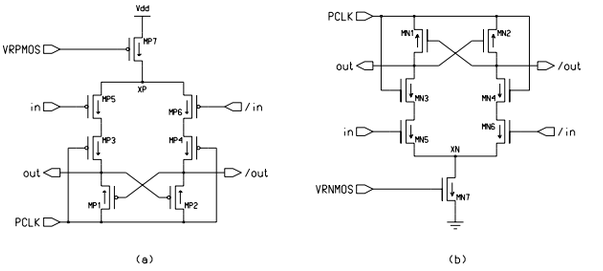

Figure 1: (a) A PMOS and (b) an NMOS inverter in SCAL.

SCAL is a partially-adiabatic logic family that is clocked by a single-phase power-clock. Low energy operation is achieved across a broad operating range by tuning a current source attached to each gate. The basic structure of a SCAL PMOS gate is shown in the PMOS inverter of Figure 1(a). This inverter comprises a pair of cross-coupled latches (MP1 and MP2), a pair of current control switches (MP3 and MP4), two function blocks (MP5 and MP6) and a current source (MP7). This current source is the main structural characteristic that differentiates SCAL from TSEL, its closest adiabatic relative. The charge flow rate through the current source is controlled by the W/L ratio of MP7. The constant voltage supply V_{dd} is required for activating the cross-coupled latches. The port PCLK is used to apply a sinusoidal power-clock Φ.

A PMOS SCAL gate operates in two phases: *discharge* and *evaluate*. The energy stored in the node out or $\overline{\text{out}}$ is recovered during *discharge*. In this phase, the power-clock Φ starts from *high* and ramps down toward *low*, pulling both out and $\overline{\text{out}}$ down toward the PMOS threshold voltage $|V_{tp}|$. The new output of a PMOS gate is computed during *evaluate*. In this phase, Φ starts rising from *low*, turning MP1 and MP2 on along the way. When the gate-to-source voltage $|V_{gsp}|$ of the current source MP7 exceeds $|V_{tp}|$, MP7 turns on and raises the voltage V_{xp} of the internal node XP. While Φ remains below $V_{\text{xp}} - |V_{tp}|$, MP3 and MP4 are conducting. Therefore, assuming that in is *high* and $\overline{\text{in}}$ is *low*, a pull-up path is created from V_{xp} to $\overline{\text{out}}$, and the voltage at $\overline{\text{out}}$ starts rising toward V_{xp}. The cross-coupled latches function as a sense-amplifier and boost the voltage difference of the two output nodes. As soon as this difference exceeds $|V_{tp}|$, MP1 turns off and the output $\overline{\text{out}}$ is charged adiabatically from that point on. When Φ exceeds $V_{\text{xp}} - |V_{tp}|$, MP3 and MP4 turn off and disconnect the functional blocks

from the outputs out and $\overline{\text{out}}$. Hence, any further changes in the inputs do not propagate to the outputs. By the end of the evaluation phase, $\overline{\text{out}}$ is charged up to the peak power-clock voltage.

The impact of the various circuit parameters on SCAL operation can be best understood by examining the equation describing the current of a MOS device in its saturation region:

$$I_{ds} \quad = \quad \tfrac{1}{2}\mu C_{ox}\,(W/L)\,(V_{gs}-V_t)^2\,, \quad V_{ds} > V_{gs} - V_t > 0$$

where I_{ds} is the drain-to-source current, V_{gs} is the gate-to-source voltage, V_t is the device threshold voltage, μ is the effective surface mobility of the carrier in the channel, and C_{ox} is the gate-oxide capacitance. From this equation, it follows that the current through the current source is controlled by the W/L ratio and V_{gs} [1]. For low-energy operation, the duration of *evaluate* should be made as short as possible by appropriately selecting the biasing voltage of the current sources. For high-speed operation, the source current should be made large enough by appropriate transistor sizing.

The main difference in the operation of SCAL and TSEL is in the control of the evaluation phase. In TSEL, a reference voltage is used to control both the duration of the evaluation phase and the value of the charging current. To ensure correct function, however, the reference voltages must be two times larger than the thresholds of the PMOS and NMOS devices. Thus, at low frequencies, the duration of *evaluate* cannot be shortened below a certain limit, and TSEL dissipation increases even when multiple reference voltages are used. On the other hand, the current flow in SCAL can be controlled by adjusting the W/L ratio of MP7, whereas the duration of *evaluate* is determined independently by selecting the biasing voltage of the current source. Thus, SCAL gates can be individually tuned to achieve minimum dissipation for low and high operating frequencies.

The inverter in Figure 1(b) shows the basic structure of a SCAL NMOS gate in which outputs are precharged high. The two phases in the operation of an NMOS gate are *charge* and *evaluate*.

3 Cascading SCAL Gates

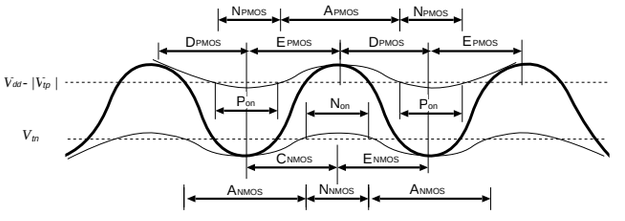

Figure 2: SCAL timing. $\mathsf{D_{PMOS}}$: PMOS *discharge* phase; $\mathsf{E_{PMOS}}$: PMOS *evaluate* phase; $\mathsf{P_{on}}$: PMOS current source on; $\mathsf{C_{NMOS}}$: NMOS *charge* phase; $\mathsf{E_{NMOS}}$: NMOS *evaluate* phase, $\mathsf{N_{on}}$: NMOS current source on; $\mathsf{A_{PMOS}}$, $\mathsf{A_{NMOS}}$: adiabatic switching for PMOS and NMOS; $\mathsf{N_{PMOS}}$, $\mathsf{N_{NMOS}}$: non-adiabatic switching for PMOS and NMOS.

SCAL cascades are built by stringing together alternating PMOS and NMOS gates. The only signal required for controlling a SCAL cascade is the power-clock Φ. The relative timing of the gates in a SCAL cascade is shown in Figure 2. At any time during the circuit's operation, either all PMOS gates evaluate and all NMOS gates charge or all PMOS gates discharge and all NMOS gates evaluate. While the current switches of the odd stages are off, the function blocks of the even stages are connected to V_{dd} or V_{ss} through the current sources and can safely evaluate their outputs. After half a cycle, while the current switches of the even stages are off, the function blocks of the odd stages are connected to V_{dd} or V_{ss} and their inputs are stable.

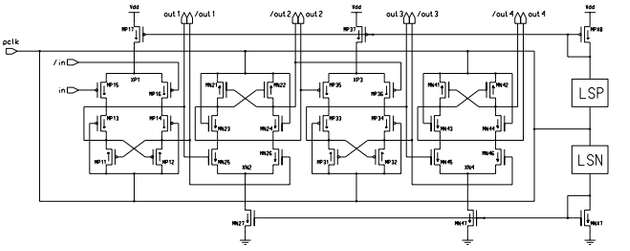

Figure 3: A pipeline of SCAL inverters with biasing circuitry.

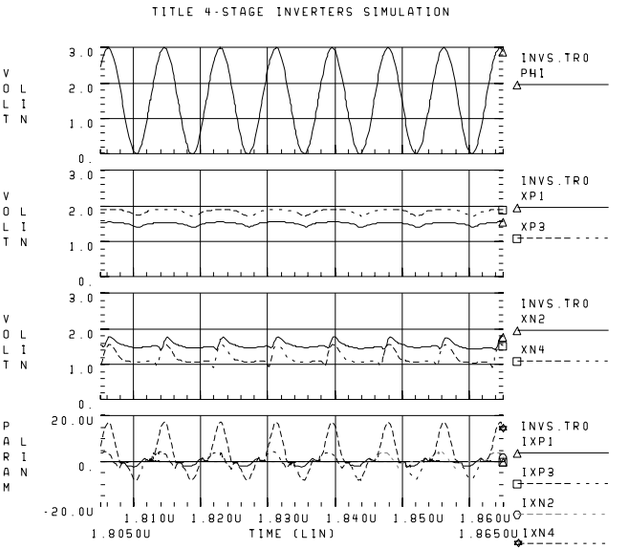

Figure 4: Waveforms obtained from HSPICE simulations of a 4-stage pipeline of SCAL inverters. From top to bottom: (1) power-clock Φ, (2) internal voltages of V_{xp1} and V_{xp3}, (3) internal voltages of V_{xn2} and V_{xn4}, (4) currents through the current sources (devices MP17, MN27, MP37 and MN47).

A PNPN cascade of SCAL inverters and the biasing circuitry for the current sources are shown in Figure 3. The blocks denoted by LSP and LSN are voltage level shifters. Figure 4 shows the internal voltages and currents through the current source for each stage of the cascade in Figure 3 when simulated at 120MHz with a 3V peak-to-peak supply voltage and a 0.5μm standard CMOS technology. In these simulations, the W/L ratio of the cross-coupled latch in each gate was $5/2$. For the function blocks, minimum size transistors were used with W/L ratio equal to $3/2$. The W/L ratios for the current sources (devices MP17, MN27, MP37 and MN47) were $1/2$, $1/4$, $2/1$ and $1/1$, respectively. The length of the *evaluate* phase is the same for every stage. The internal voltages V_{xp1}, V_{xn2}, V_{xp3}, and V_{xn4} and the internal currents I_{xp1}, I_{xn2}, I_{xp3}, and I_{xn4} are proportional to the W/L ratios of the current sources. These voltages and currents affect the energy dissipation of the SCAL structures. As the W/L ratio decreases, the current is reduced. Symmetrically, as the W/L ratio increases, the current associated with the non-adiabatic event in the gates increases. For each gate, the optimal ratio can be achieved independently of the duration of the non-adiabatic evaluation. Therefore, energy dissipation can be reduced by using several current source sizes as opposed to just one.

4 Simulation Results

In this section, we present HSPICE simulation results for pipelined 4-bit CLAs that we developed in SCAL, TSEL, 2N-2P, PAL, and static CMOS. Our circuits were designed using a standard 0.5μm CMOS technology and were simulated with distributed RC parameters that were extracted from layout. Our simulations accounted for the dissipation of the gates and internal clock lines but did not include the energy consumed on the external clock distribution network or the power-clock generator.

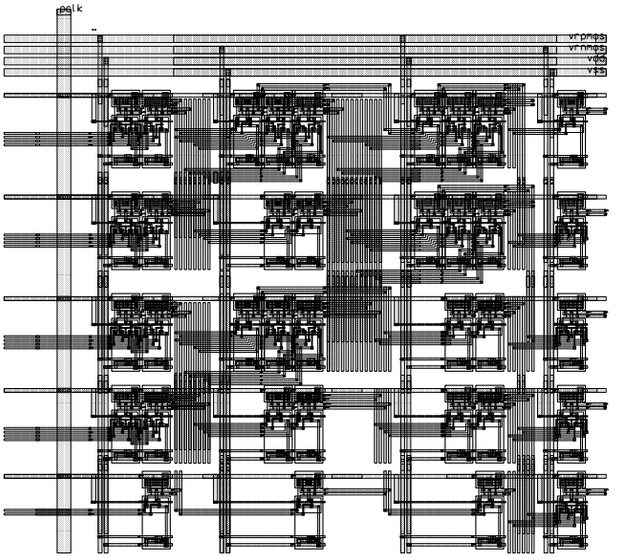

Figure 5: Layout of 4-stage pipelined 4-bit CLA in SCAL.

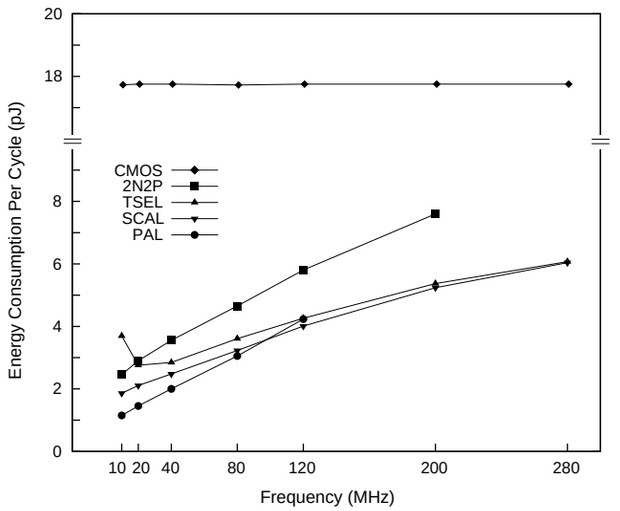

Figure 6: Energy consumption vs. frequency for 4-bit CLA.

The layout of our SCAL CLA is shown in Figure 5. The W/L ratio of each current source was selected among the values 1/8, 1/4, 1/2 and 1/1 according to the output capacitive loads of its gate and the operating frequency. Figure 6 gives the per-cycle energy consumption of our designs as a function of their operating frequency for a uniformly distributed random input sequence. The peak power-clock voltage was 3V, and each primary output was connected to a 60fF load. As expected, the energy consumption of the static CMOS implementation does not vary with the operating frequency. SCAL is less dissipative than 2N-2P and TSEL for the entire operating regime. Moreover, it is more efficient than PAL for operating frequencies above 100MHz. Below 100MHz, SCAL is still competitive with PAL and is no more than 50% more dissipative at 10MHz. SCAL operates at full logic swing for frequencies up to 280MHz. At 280MHz, it is about 3 times more energy-efficient than static CMOS. 2N-2P breaks down at 200MHz. At that point, TSEL and SCAL are 1.5 times more efficient than 2N-2P.

5 Summary and Ongoing Work

We have described an adiabatic logic that functions efficiently across a wide operating range. Our logic requires a single power-clock phase for its operation and avoids numerous problems associated with multiple phases, including increased energy dissipation and layout complexity in the clock distribution network, clock skew, and multiple AC power supplies. Its efficient operation is based on a current source that can be tuned to control the rate of charge flow into or out of the gate during evaluation.

We are currently evaluating the performance of SCAL under voltage scaling [5]. Preliminary results from layout simulations of CLAs indicate that SCAL can operate with very low supply voltages and is significantly more efficient than corresponding CMOS, 2N-2P, TSEL, and PAL designs.

Acknowledgments

This research was supported in part by a Young Investigator Award from the US Army Research Office under Grant No. DAAG55-97-0395.

References

[1] P. E. Allen and D. R. Holberg. *CMOS Analog Circuit Design*. Oxford University Press, 1987.

[2] W. C. Athas, L. J. Svensson, J. G. Koller, N. Tzartzanis, and Y. Chou. Low-power digital systems based on adiabatic-switching principles. *IEEE Transactions on VLSI Systems*, 2(4):398–406, December 1994.

[3] J. S. Denker. A review of adiabatic computing. In *Proceedings of the 1994 Symposium on Low Power Electronics/Digest of Technical Papers*, pages 94–97, October 1994.

[4] S. Kim and M. C. Papaefthymiou. True single-phase energy-recovering logic for low-power, high-speed VLSI. In *Proceedings of International Symposium on Low-Power Electronics and Design*, August 1998.

[5] S. Kim and M. C. Papaefthymiou. Low-energy adder design with a single-phase source-coupled adiabatic logic. 1999. Submitted for Publication.

[6] M. C. Knapp, P. J. Kindlmann, and M. C. Papaefthymiou. Implementing and evaluating adiabatic arithmetic units. In *IEEE 1996 Custom Integrated Circuit Conference*, pages 115–118, 1996.

[7] A. Kramer, J. S. Denker, B. Flower, and J. Moroney. 2nd order adiabatic computation with 2N-2P and 2N-2N2P logic circuits. In *1995 International Symposium on Low Power Design*, pages 191–196, 1995.

[8] D. Maksimovic, V. G. Oklobdzija, B. Nikolic, and K. W. Current. Clocked CMOS adiabatic logic with integrated single-phase power-clock supply: Experimental results. In *Proceedings of International Symposium on Low Power Electronics and Design*, pages 323–327, August 1997.

[9] V. G. Oklobdzija and D. Maksimovic. Pass-transistor adiabatic logic using single power-clock supply. *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, 44(10):842–846, October 1997.