Validation and Test Generation for Oscillatory Noise in VLSI Interconnects

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Abstract: Inductance of on-chip interconnects gives rise to signal overshoots and undershoots that can cause logic errors. By considering technology trends, we show that in 0.13 μm technology such noise in local interconnects embedded in combinational logic can exceed the threshold voltage. We show the impact of such noise on different kinds of circuits. The magnitude of this noise can increase due to process variations. We present an algorithm for generating vectors for validation and manufacturing test to detect logic-value errors caused by inductance induced oscillation. To facilitate the vector generation method, we have derived analytical expressions, as functions of rise and fall times for (i) the magnitude of overshoots and undershoots, and (ii) the settling time, i.e., the time required for the circuit response to settle to a bound close to the final value.

1 Introduction

Advancements in integrated circuit technology have led to an increase in switching speeds of digital circuits. This increase is the primary reason why inductance induced noise (e.g., oscillation, delay, crosstalk) is beginning to cause chips to fail. Thus, we now see a great interest in inductance of on-chip signal lines [6].

Researchers have investigated validation and test issues related to high speed switching noise in integrated circuits. Validation and test issues for capacitive crosstalk were discussed in [4],[5],[10]. Inductive coupling effects between bus lines were considered in [12]. *In this paper, we present procedures for generating validation and test vectors to detect functional errors caused by overshoots and undershoots due to inductance induced oscillation.* Oscillatory noise has been discussed in [14]. *However, any previous attempt to generate test vectors for such noise is not known.* This mixed-signal test generator uses a PODEM-like approach [1] and extends an existing test generator for crosstalk faults [4] by (i) considering conditions for excitation of inductance induced oscillations that reduce backtracking, and (ii) relaxing propagation conditions that subsequently increase the solution space.

In future, signal overshoot and undershoot are expected to increase in magnitude and occur more frequently. This noise may propagate to a primary output or a latch input and create logic-value (permanent) errors. By considering technology trends we have shown that such noise in local interconnects embedded in combinational logic block may exceed the threshold voltage in 0.13 μm technology. *This motivates the validation problem.* The impact of process variation on noise has been discussed in [11]. The severity of the impact of process variation on noise depends on the aggressiveness of a design. For example, a technique to design interconnects that reduces the output delay by a large amount by causing a small overshoot has been presented in [2]. An aggressive design that employs such a trade-off may exhibit a large overshoot or undershoot in a fabricated circuit due to process variation. *This motivates the test generation problem.*

To facilitate the proposed test generation method, we have derived analytical expressions for (i) the magnitude of overshoots and undershoots, and (ii) the settling time, i.e., the time required by the circuit response to settle to a bound close to the final value. The analytical expressions can also be used by a designer to guide design decisions and help reduce the number of circuit simulations that must be performed during design. We have modeled the input as an exponential function with arbitrary rise times (time required by the input to change from 10% to 90% of its final value) and fall times, in contrast to previous researchers who have used a step input approximation [7], [18]. Using step input to model the magnitude of oscillatory noise is less accurate than using an exponential input and any design that attempts to eliminate all noise problems via step input analysis will be conservative.

2 Circuit Model

Inductance is associated with a current loop. In a VLSI chip, when a single signal line switches, numerous current loops are formed through the interconnect substrate, power and ground lines [16].

A conventional transmission line assumes only one current return path. We can use conventional transmission line analysis if we assume that there is no transient potential drop on the return paths and thus lump them together as a single terminal. The interconnect circuit and model are shown in Fig. 1. The driver resistance is modeled as a constant linear resistance, denoted by R_{source}. The receiver can be one of the following: (i) a static gate, (ii) a transmission gate, (iii) a pass transistor, or (iv) a domino

gate. The load can be modeled as a capacitance (in the case of a static inverter, domino gate, and non-conducting pass transistor or transmission gate) or a resistance (conducting pass transistor or transmission gate) and is assumed constant and is denoted by C_{load} or R_{load}. One section of the transmission line is shown in the figure, where r, l and c are the resistance, inductance and capacitance per unit length. Since the resistance of the dielectric is high, the shunt conductance in a conventional transmission line model is ignored. The symbols *IN*, *NE*, *FE* and *OUT* refer to the input to the driving buffer, the near end of the interconnect, the far end of the interconnect and the output of the receiver, respectively.
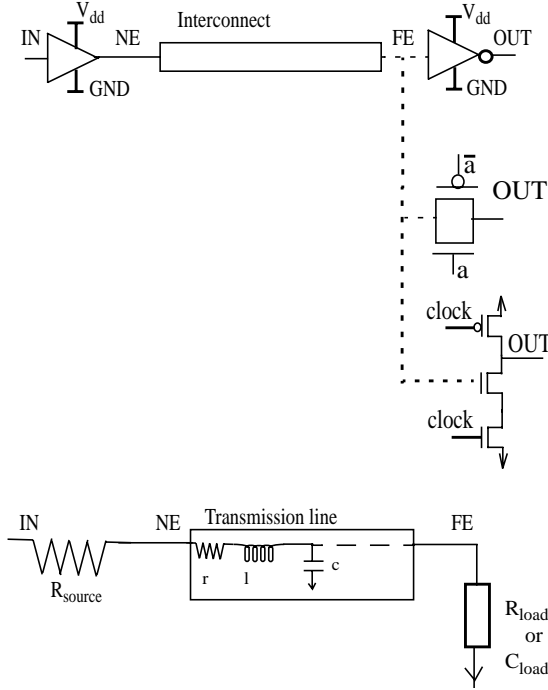

Figure 1: Interconnect circuit and model.

3 Motivation

3.1 Oscillatory noise

The oscillatory response is created by the mismatch of impedances between the interconnect and the driver, and the interconnect and the receiver, when the attenuation of the interconnect is not high enough to damp the oscillation. For a rising response, an *overshoot* occurs if its magnitude at some instance of time is larger than the final stable value. An *undershoot* occurs if, once the response initially reaches a voltage equal to its steady state value, it drops below this value. The definitions for a falling response are similar.

The *settling time* is the time after which the oscillatory circuit response does not deviate from its final value by more than a certain fraction of the final value [9]. The 50%-input to 50%-output change is a popular delay metric for RC interconnects in VLSI circuits. By this criterion, the output of a RLC interconnect may have less delay than an RC interconnect, but the receiver gates may switch several times due to signal oscillation.

In this scenario, the settling time is a more meaningful delay criterion than 50%-input to 50%-output delay.

We conducted an experiment to see how the magnitudes of overshoot, undershoot and settling time change with changes in rise (fall) times of the input stimulus. The interconnect model in Fig. 1 with a capacitive load is used for this study. To justify the parameters used in our experiments we looked at technology trends predicted by the SIA Roadmap and MOSIS [13], [15].

Year	1997	1999	2001	2003
Feature size (nm)	250	180	150	130
Logic Vdd (V)	1.8-2.5	1.5-1.8	1.2-1.5	1.2-1.5
On-chip local clock (GHz)	.75	1.25	1.5	2.1
Microprocessor chip size (mm^2)	300	340	385	430
Line Thickness (μm)	.45	.324	.3	.273

Table 1: Projections from SIA Roadmap.

Table 1 shows projections on the power supply voltage, on chip clock frequency, microprocessor chip size and interconnect thickness from the SIA Roadmap [13]. Table 2 shows a few parameters that have been collected from MOSIS process files along with the projections for the 0.13 μm technology (shaded row) using the collected data [15]. Columns 2 and 3 show the sum of area and fringe capacitances of the N-active and the P-active layers. Column 4 shows the substrate capacitance of the third metal layer. Column 5 shows the product of the mobility and the gate oxide capacitance. The channel resistance of a transistor is shown in Column 6 and is calculated as

$$R = \frac{k}{\mu_0 C_{ox}(V_{gs} - V_t)}\left(\frac{L}{W}\right),$$ where k is a constant and considered equal to 1, V_{gs} is the gate to source voltage, V_t is the thresh-

Feature Size (μm)	N-active capacitance (aF/μm^2)	P-active capacitance (aF/μm^2)	Metal 3 capacitance (aF/μm^2)	$\mu_0 \cdot C_{ox}$ (μA/V^2)	Channel Resistance (Ω)	Logic Vdd (V)	Threshold Voltage (V)
1.2	357	463	--	69	52	5	1
.8	755	1032	--	106	34	5	1
.5	798	1013	12	112	32	5	1
.35	826	1072	7	176	31	3.3	.7
.13	1100	1100	5	496	30	1.2	.24

Table 2: Some parameters from MOSIS process files.

old voltage, and L and W are the length and width of the transistor, respectively. The *W/L* ratio is chosen to be 70 (a fast driver), and its resistance estimated as 30 Ω . Based on the data collected for 1.2 μm, 0.8 μm, 0.5 μm, 0.35 μm technologies, each of the N-active and the P-active capacitances in 0.13 μm technology are estimated to be 1100 aF/μm^2. The load capaci-

tance of a receiver with an *n*-transistor whose *W/L* ratio is 100 and a *p*-transistor whose *W/L* is 200 is calculated to be about 5 fF. The distribution of interconnect lengths in a chip is bimodal, and assuming that the length of each edge of a chip is 2 cm (Table 1), the distribution has two peaks, one at around 2500-3000 μm (intramodule) and another at around 15000 μm (inter-module) [8]. We assume an interconnect length of 2500 μm. We further assume that its width is 3μm, and its thickness is 0.27 μm (Table 1). Assume that the interconnect material is copper with a conductivity of 58.8/Ω-μm and resistance per unit length of 0.02 Ω/μm. The substrate capacitance of the third metal layer is estimated to be 5 aF/μm^2 (Table 2). The interconnect is assumed to be on the third metal layer and therefore its capacitance per unit length is 0.015 fF/μm. The value of inductance per unit length depends on the design of the power-ground mesh (since current returns through the mesh) and therefore a single value cannot be estimated for all designs. We will assume a value of 1 pH/μm. Inductance values with similar and higher magnitudes have been reported in literature [6]. It should be noted that resistance and inductance values are slightly increased and decreased respectively, due to frequency dependent skin and proximity effects [20]. If skin and proximity effects are required to be modeled, then frequency dependent models may be used. Not modeling skin and proximity effects does not alter the qualitative understanding of this phenomenon. The magnitude of the power supply voltage is assumed to be 1.2 V (Table 1). Assuming a clock frequency of 2 GHz (Table 1), the rise time can be approximated as 50 ps (= (1/10)*(1/2 GHz)). For this experiment, the input was modeled by an exponential function and the rise time was varied from 25 ps to 100 ps in steps of 25 ps.

Several simulations were performed using *Spice3*. Fig. 2 shows the response at the far end and Table 3 summarizes the results. The settling time measures the time for the response to reach within 10% of its final value (i.e., between 0.9 Vdd and 1.1 Vdd) starting from its initial value. We see that with an increase in input rise time, initially the settling time decreases and then increases. This implies that the rise (fall) time of the input stimulus should ideally be that which corresponds to an optimum settling time (shaded rows). Assuming that the threshold voltage is 0.24 V (=0.2Vdd), the magnitude of the overshoot in the first case is larger than the threshold voltage. The undershoots in the first two cases are greater than the threshold voltage. The overshoots and undershoots are absent if the input signal rise time is 75 ps or greater.

We see that the faster the input rise time, the higher is the magnitude of the noise. Therefore, our test generation method will attempt to achieve objectives that result in fast rise (fall) times at the interconnect line being targeted.

3.2 Noise Effects

Assume that a static inverter is driving a transmission line that has one of the following three receivers, a transmission gate, a domino latch, or a static inverter. We will see how the outputs differ for each of these cases.

An undershoot in case of a rising response and an overshoot in case of a falling response should be avoided at the far end of the interconnect (FE in Fig. 1), especially if their magnitudes are greater than V_{tp} and V_{tn}, respectively, where V_{tp} and V_{tn} are the threshold voltages of the *p* and *n* transistors of the gate at the far end. Such a situation may propagate the noise.
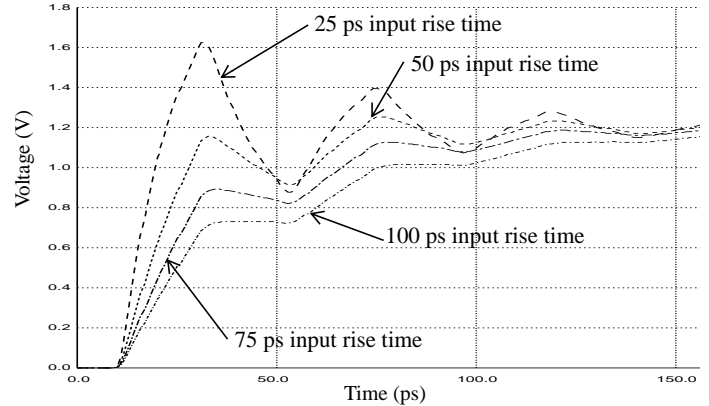

Figure 2: Circuit response at FE with rise time variation at input IN.

Input rise time (ps)	Maximum overshoot (V)	Maximum undershoot (V)	Settling time (ps)
25	0.42	0.32	100
50	0.06	0.28	63
75	--	--	70
100	--	--	106

Table 3: Characteristics at the FE of the line.

Overshoots and undershoots do not propagate via static CMOS logic, although an overshoot (undershoot) at the input of the static inverter makes the falling (rising) transition at its output faster by a small amount.

There are, however, families of logic that are adversely affected by overshoots and undershoots. For example, in the case where FE drives the source/drain of a transmission gate, assume that the gate input of a *n* pass transistor is at 0 V. An undershoot of magnitude greater than the threshold voltage of the *n*-transistor at FE will discharge the charge stored at its output [21]. This is because the gate to source voltage exceeds the threshold voltage. Similarly, an overshoot at the source of a *p*-transistor can cause it to discharge.

The following simulations are done using HSPICE and 0.25 μm process files from MOSIS. (We do not have access to more recent technology data.) In this technology, the power supply voltage is 2.5 V and the threshold voltage is 0.6 V. We have increased the magnitude of the inductance to increase the magnitude of the oscillation. In later technologies, the magnitude of the threshold voltage will be lower, and therefore, a more subdued oscillation may have a similar impact. The transmission line resistance, capacitance and length are 0.02 Ω/μm, 15 aF/μm and 5000 μm, respectively. A fast driver is used in each case and the transmission line inductance is discussed for the specific simulation.

Fig. 3 shows the results at the output of a domino latch that is sensitive to an overshoot in the case of a falling response. The input to the evaluation transistor has a falling transition just before the clock goes high, such that the oscillation persists after the clock changes. The magnitude of the overshoot is high

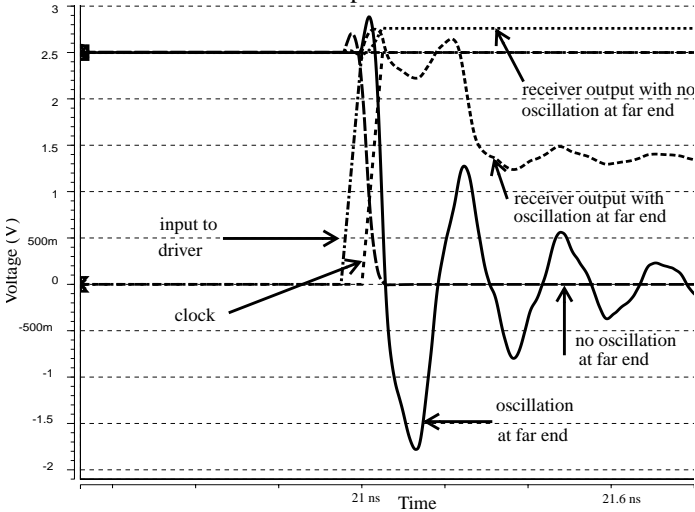enough to degrade the output voltage level. The magnitude of the interconnect inductance is 5 pH/um.

Figure 3: Impact of oscillation on domino latch.

Fig. 4 shows the results for a transmission gate that discharges the stored charge, even though the gate inputs to the n and p transistors of the transmission gate are low and high respectively. This occurs because the magnitude of the undershoot is greater than the threshold voltage of the n-transistor. Again, the magnitude of the interconnect inductance is 5 pH/μm.
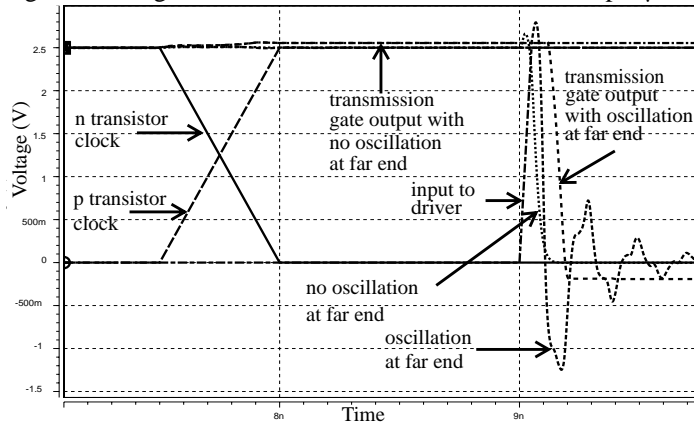

Figure 4: Impact of oscillation on transmission gate.
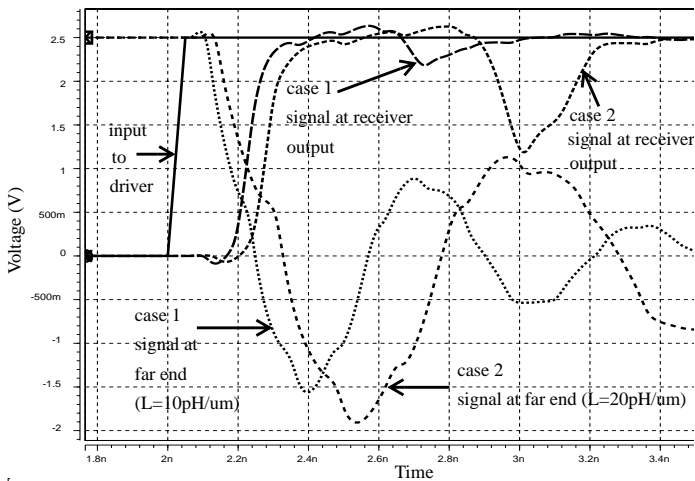

Figure 5: Impact of oscillation on static inverter.

Fig. 5 shows the noise at the far end of two transmission lines that have identical receivers. The first transmission line has an inductance of 10 pH/μm and the second 20 pH/μm. The noise at the output of the receiver has a higher magnitude in the second case.

It appears that pass transistors and domino logic gates are more susceptible to noise than static inverters.

4 Process Variation

The impact of process variations on inductance can be assumed to be negligible because the area of the loops are large compared to changes in dimensions due to process variations. However, oscillatory response can still vary significantly due to variations in other circuit parameters. We illustrate this with the example described in Section 3.1. Table 4 shows the nominal values and the values under process variations. (Process variation data for newer technologies are not available to us.) The percentage variations are assumed to be the same as that in the 0.8 μm process reported in [11]. The percentage variations cover 98% of all measured data points implying that process variation effects can be more severe than that reported here.

Parameters		% Variation	Minimum	Nominal	Maximum
Source Resistance (Ω)		±15	25.5	30	34.5
Load Capacitance (fF)		±5	4.75	5	5.25
Trans. Line	r (Ω/μm)	±15	0.017	0.02	0.023
	c (fF/μm)	±30	0.0105	0.015	0.0195
Maximum undershoot (V) (% Variation about nominal)			0.34 (21)	0.28	0.22 (21)
Settling time (ps) (% Variation about nominal)			69 (10)	63	87 (38)

Table 4: Impact of process variation.

We see that for a 2500 μm long line, the magnitudes of undershoot and settling time change significantly with variation in parameters (shaded rows). The magnitudes of the maximum overshoot do not change significantly for this specific example and are not shown. This implies that a fabricated design may have significant overshoot and undershoot even if it is designed to suppress such noise. Assuming that the threshold voltage is 0.24 V, the undershoot for the combination of minimum values of parameters is much larger than the threshold voltage and can cause a logic-value error. Hence, it is necessary to treat this situation as a test problem.

5 Analytical Model of Interconnect

In this section we derive an (approximate) expression that describes the response at node FE of the circuit in Fig. 1. We also determine the magnitudes and times of occurrences of the undershoots and overshoots and the settling time. These expressions can be used in a test generation process. They can also be used to guide the design process.

Let the length of a transmission line be h, and its resistance, capacitance and inductance per unit length be r, l and c. Let $R = rh$, $C = ch$ and $L = lh$. The propagation constant of a transmission line is $\gamma = \sqrt{(R + sL)sC}$ and its characteristic impedance is

$Z_0 = \sqrt{(R + sL)/(sC)}$. Let its source resistance be R_s and load impedance be Z_l. The transfer function of this network is given by [7]

$$H(s) = \left[\left[\cosh(\gamma h) + \frac{R_s}{Z_o}\sinh(\gamma h)\right] + \frac{1}{Z_l}[Z_0\sinh(\gamma h) + R_s\cosh(\gamma h)]\right]^{-1}.$$

Taking the Maclaurin series expansion of the denominator about $s=0$, we determine the first two moments of the expression M_1 and M_2, where $M_1 = R_sC + R_sZ_l + RC/2 + RZ_l$, and $M_2 = R_sRC^2/6 + R_sRCZ_l/2 + R^2C^2/24 + R^2CZ_l/6 + LC/2 + LZ_l$. We will approximate the transfer function by these first two moments since these are the dominant ones. Thus, the approximate transfer function can be written as $H'(s) = 1/\left(1 + M_1s + M_2s^2\right)$. Assuming that the input is of the form $1 - e^{-at}$, the output can be written as $C(s) = H'(s)(1/s - 1/(s + a))$. We can rewrite $H'(s)$ as $H'(s) = w^2/(s^2 + 2\zeta ws + w^2)$, where $w = 1/(\sqrt{M_2})$ and $\zeta = M_1/(\sqrt{M_2})$. Here, ζ and w are the approximate damping factor and the natural frequency of the system [9]. Since we are addressing oscillatory noise, we will assume an underdamped system, hence $\zeta < 1$ ($\zeta = 1$ and $\zeta > 1$ correspond to critically damped and overdamped systems, respectively). By means of the inverse Laplace transform, the output is

$$C(t) = 1 - Ae^{-at} - Aae^{-\sigma t}\frac{\sin(w_dt)}{w_d}$$

$$-(1 - A)\frac{e^{-\sigma t}}{\sqrt{1 - \zeta^2}}\left(\sin(w_dt)\zeta + \cos(w_dt)\sqrt{1 - \zeta^2}\right),$$

where $\sigma = \zeta w$, $w_d = w\sqrt{1 - \zeta^2}$, and

$$A = w^2/(w^2 - 2\zeta wa + a^2) \quad .$$

To determine the time of occurrence of the overshoots and undershoots, we determine the value of t for which $\frac{d}{dt}C(t)$ is 0. Because the input has almost reached its final value when the peak of the overshoot or undershoot occurs, we will assume that Ae^{-at} is equal to 0 when this peak occurs. This assumption helps to determine a closed form solution. The overshoots and undershoots occur at $t = (n\pi + \theta)/w_d$, where n=1,2,3,...,

$$\theta = ArcCos\left(p/\left(\sqrt{p^2 + q^2}\right)\right),$$

$p = (1 - A)\left(\sigma^2/w_d + w_d\right) + (Aa\sigma)/w_d$ and $q = Aa$. By substituting these values of t into $C(t)$, we can determine the magni-

tudes of the overshoots and undershoots. The settling time can be found by determining when the exponential decay term in $C(t)$ is within a bounded value, and can be expressed as

$$t = ((-1)/\sigma)\log\left[(b/100)\cdot\left(\sqrt{1 - \zeta^2}\right)/\left(\sqrt{K_1^2 + K_2^2}\right)\right],$$

where b is a bound, $K_1 = -\zeta - \left(Aa\sqrt{1 - \zeta^2}\right)/w_d + A\zeta$, and

$K_2 = (A - 1)\sqrt{1 - \zeta^2}$. The magnitude of the settling time may be in error by at most half the period of oscillation.

In Table 5 we compare the values predicted by our model with those determined by *Spice3* simulations, for the case where the bound $b=10$. The circuit parameters and the rise times are shown in the first and second columns of Table 5. The maximum magnitude of the error is about 25%. If one is interested in a more accurate model, one may consider additional moments of the transfer function. In spite of the error, this is a better approximation than the values determined using a lumped parameter approximation.

This approximation is also more accurate than a step input approximation. For example, for the set of parameters shown in Table 5 and a step input, and considering the first two moments of the transfer function, the approximate magnitudes of the overshoot, undershoot and settling time are 0.55 V, 0.31 V and 979 ps, respectively. If the input has a rise time of 250 ps, the errors in approximating those quantities are 67%, 48% and 21%. In comparison, the errors predicted by our model are 24%, 24% and 2%, respectively.

To see how using the step input approximation leads to a conservative design, let us assume that in the first example, an overshoot greater than 0.1 V cannot be tolerated, and that it is decided to change the source resistance alone to satisfy this constraint. The step input approximation suggests using a source resistance of magnitude 72 Ω. Based on the exponential model for the input, a 43 Ω source resistance is sufficient. Via *spice3* simulations for a 72 Ω and a 43 Ω source resistance, the settling times for the response to reach 0.9 V are 309 ps and 251 ps, respectively. Therefore, modifying the design on the basis of a step input approximation increases the delay by 58 ps (23%).

6 Procedure for Test Generation

The process of validation deals in part with generating and simulating test vectors whose application excites the worst case noise. If this noise creates an error, the circuit should be redesigned. Alternatively, tests can be generated to test fabricated chips to identify noise induced errors missed during validation and the effects of process variation. In this section we address the problem of generating tests to be used for both design validation and testing. The problems targeted are the effects of oscillation i.e., overshoot and undershoot that may cause an erroneous value to be stored in latches/flip-flops. We refer to these noise effects as "faults". These faults may not be detected by conventional two pattern tests. We will generate tests using an ATPG system that is

Circuit Parameters	Rise time (ps)	First Overshoot				First Undershoot				Settling time (ps)	
		Magnitude (V)		Time of occurrence (ps)		Magnitude (V)		Time of occurrence (ps)			
		Spice	model (%error)	Spice	model (%error)	Spice	model (% error)	Spice	model (% error)	Spice	model (% error)
R=.003Ω/μm L=1 pH/μm	25	0.6	0.55 (8.3)	275	261 (5)	0.36	0.3 (17)	486	511 (5)	966	985 (2)
C=.1 fF/μm Length=1cm	50	0.58	0.53 (8.6)	250	272 (4.8)	0.35	0.29 (17)	421	522 (24)	954	984 (3)
Rs=10 Ω Cload=.1 pF Vdd=1 V	250	0.33	0.25 (24)	318	335 (5.3)	0.21	0.16 (24)	543	585 (8)	812	793 (2)

Table 5: Comparison of SPICE simulation and model.

an extension of an existing mixed signal test generator for crosstalk [5].

It is assumed that the layout has been scanned and a list of target interconnects susceptible to oscillation has been generated. We also assume that the circuit is combinational with static CMOS logic gates. A sequential circuit can be decomposed into blocks of combinational logic and the test generation method can be applied to each combinational logic block with the assumption that its inputs (which are primary inputs or flip-flop outputs) are deterministically controllable and outputs (which are primary outputs, or flip-flop inputs) are observable. This model is the same one used in most papers on delay testing.

6.1 Test Generation Example

In this section we illustrate the requirements of the ATPG algorithm with the aid of an example. We determine a test for the undershoot generated during the rising transition on line 16 in Fig. 6. Let us assume that the primary input transitions occur simultaneously. Also assume that each gate has a delay of 100 ps and the clock sampling time at the output is aggressively set at 325 ps.
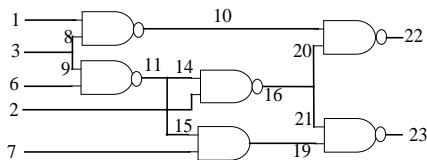

Figure 6: Example to illustrate the vector generation algorithm

The undershoot on line 16 must occur at 225 ps for its effect to reach the output at the sampling time. The rising transition on line 16 can be achieved in several ways. Among those assignments at the inputs that produce a rising transition on line 16, a falling transition on line 2 is avoided, because it will cause the signal to arrive on line 16 at 100 ps and therefore the undershoot on line 16 will occur a little after 100 ps. If we use this assignment, the undershoot will propagate to an output a little after 200 ps and the signal will stabilize before the clock sampling time. As a result, the fault will not be detected. Thus, line

2 is assigned the value of static 1. This demonstrates that in our ATPG algorithm, we need a method to determine when an undershoot or an overshoot must occur so that it propagates to an output at the clock sampling time. We will define *signal arrival time* and *response arrival time* in order to achieve this. The rising transition on line 16 can be achieved by means of a falling transition on line 11, which can be achieved only by having a rising transition on both lines 3 and 6. Thus, by means of *backtracing* from line 16, we have determined values on lines 3, 6 and 2, that results in *excitation* of the undershoot. The magnitude of the undershoot can be calculated by the procedure described in Section 5.

Next, we want to determine conditions for *propagation* of the undershoot to an output. By using the equivalent inverter model which replaces a logic gate by an inverter of equivalent *p* and *n* transistors [4], we can determine whether the undershoot propagates to lines 22 and 23, and if so, their magnitudes after propagation. Suppose that the gates on line 22 and 23 amplify the noise and can potentially cause an erroneous value to be latched, and that it is decided to propagate the noise to line 23. A static 1 value or a rising transition on line 19 is required for this purpose. A rising transition on line 19 can be achieved by a rising transition on one input of the AND gate and a static 1 value on the other, or by rising transitions on both inputs. A static 1 value on line 19 can be achieved by having static 1 values on both of its inputs. Neither the static 1 value nor the rising transition on line 19 is achievable as we had assigned a falling transition on line 11. To resolve this *conflict*, we are required to *backtrack* from our last assignment. We now try to propagate the undershoot to line 22. This requires a static 1 value or a rising transition on line 10. A static 1 value on line 10 can be achieved by providing a static 0 value on line 1. Thus, the test that we determined is as follows: static 0 value on line 1, static 1 value on line 2, and rising transitions on lines 3 and 6; there is no requirement on line 7.

Similarly, to test for the overshoot generated by the falling transition on line 16, we need rising transitions on both lines 11 and 2. The rising transition on line 11 can be achieved in one of the following ways: (i) a falling transition on line 3 and static 1 on line 6, (ii) a falling transition on line 6 and static 1 on line 3,

and (iii) falling transitions on both lines 3 and 6. In section 3.1, we saw that the faster the transition, the larger the magnitude of the noise. Therefore, we will opt for the third alternative. This will result in a faster transition on line 11 and consequently, more noise on line 16. The test can be propagated by a static 0 value on line 1, as before.

The two pattern tests generated by the above procedure can be applied using the slow-fast application scheme commonly used to apply robust path delay tests.

6.2 Need for a new test methodology

In this section we illustrate, by means of the circuit in Fig. 6, the reason why oscillation faults cannot be detected by conventional two pattern tests.

Assume that the undershoot during the rising transition on line 10 is to be tested. Let us further assume that the undershoot has a magnitude that results in an error only when there are falling transitions on both lines 1 and 3 (two falling transitions at the input of the NAND gate result in a faster rise time at the near end of line 10, compared to one falling transition). Consider the tests for robust path delay faults that result in a rising transition on line 10 [19]. One test has a falling transition on line 1 and a static 1 value on line 3, the other test has a falling transition on line 3 and a static 1 value on line 1. Thus, robust path delay tests may not cover oscillation faults.

To see the differences with tests for transition faults, let us assume that rising transition on line 16 is to be tested. This may be tested by a falling transition on line 2 and static 1 value on line 11. However, we saw in the previous section that a falling transition on line 2 cannot be a test for the undershoot generated by the rising transition on line 16.

Crosstalk occurs when one signal line (affecting line) induces an undesired voltage level on another (victim line). Crosstalk test patterns cannot be used for our purpose because these patterns create a fast transition at an affecting line and propagate noise effects from the victim line to an output [4]. Test patterns for *Iddq* testing do not propagate fault effects from fault sites and therefore do not detect the noise effects being considered [17]. Also, test vectors for ground bounce are not sufficient because the objective of these vectors is to maximize the transient switching current [3].

6.3 ATPG Requirements

6.3.1 Fault Excitation

The initial objective of the test generation procedure is to set desired values to excite the oscillatory response. Let *I* be an assignment on the inputs that results in the required transition. *I* can be found using a backtrace procedure. For each transition on the target interconnect due to *I*, we determine its *signal arrival time,* t_a, and its *rise (fall) time*.

Definition: The *signal arrival time,* for a rising transition is defined as the time when the transition reaches 10% of its final value. The definition for a falling transition is similar.

The rise time of a signal is the time required for the signal to change from 10% to 90% of its final value. The signal arrival time of a circuit input is defined to be zero, and for a logic gate, the signal arrival time at its output can be determined in a straightforward manner. A few examples of calculating the signal arrival times for an AND gate are shown in Fig. 7. The rise (fall) time can be determined by converting a CMOS gate into an equivalent inverter and applying transient response analysis to the equivalent inverter [4]. In this way, the signal arrival time and rise (fall) time of a transition at the target interconnect can be approximated for an input assignment *I*. Whenever we have a choice, we will choose the input assignment that results in the fastest rise (fall) time at the target interconnect, as it increases the oscillatory noise. The noise can be computed at the target interconnect by means of the procedure described in Section 5. Next, we define the response arrival time to ensure that we consider only those assignments on inputs that can potentially cause a failure.

$$t_a(g) = \max(t_a(x), t_a(y)) \qquad t_a(g) = \min(t_a(x), t_a(y))$$

$$t_a(g) = t_a(x) \qquad t_a(g) = 0$$
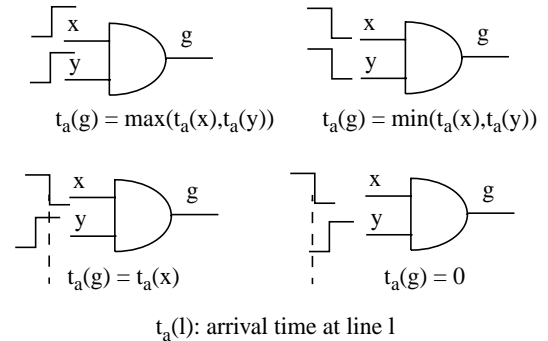
$t_a(l)$: arrival time at line l

Figure 7: Calculation of signal arrival time

Definition: The *response arrival time* of a primary output is *the* clock sampling time. The set of response arrival times at a gate's inputs is obtained by subtracting the gate delay from the set of response arrival times at its output. Each line that can be reached from more than one output can have more than one response arrival time.

Starting with each output, we determine the response arrival times at the target interconnect. The overshoot or undershoot must occur at one of these times to create a functional failure. The set of response arrival times can be found by depth first search. In determining signal arrival times and response arrival times, it is assumed that the wire delay is lumped with the gate delay. Correlating the signal arrival time and the response arrival time at a target interconnect reduces the amount of backtracking. For example, if the largest signal arrival time is less than the smallest response arrival time, then no test exists.

6.3.2 Fault Propagation

Each element in the set of response arrival time corresponds to a path from the target interconnect to outputs. Only these paths have to be searched for propagation of the noise. Each oscillatory transition to a controlling value can be propagated through a gate by applying static non-controlling values at the off-path inputs. For an oscillatory transition to a non-controlling value, we can relax the off-path conditions. Such transitions to a noncontrolling value can be propagated by using transitions to noncontrolling values on all off-path inputs. The transitions to a noncontrolling value on the off-path input of a two-input gate can occur (i) before, (ii) after, or (iii) during the oscillation. In the first case, the oscillatory noise can be propagated through the gate. In the second case, if the noise were to create an error at an output, the transition on the off-path input would create an addi-

tional delay at the same output and therefore, cause a delay fault. This is because the oscillation precedes the off-path transition. In the third case, if the oscillation were to create an error at an output, the off-path transition does not reduce the chances of the error. Relaxing the propagation condition for an oscillatory transition to a non-controlling value increases the solution space.

The noise at the output of a receiver can be determined from the noise at its input and the transfer function of the receiver. The transfer function of a static gate can be determined by the equivalent inverter method [4]. Transfer functions for pass transistors, transmission gates, and domino gates and extension to sequential circuits are under investigation.

7 Conclusions

Inductance of on-chip interconnects gives rise to overshoots and undershoots. We have shown that in future technologies the magnitude of this noise may be greater than the threshold voltage and thus may cause logical errors. We have shown how CMOS logic gates are affected by such noise, and the magnitude of this noise can increase due to process variations. We have described procedures for generating validation and test vectors to detect functional errors caused by inductance induced oscillation. To facilitate the proposed test generation method, we have derived analytical expressions for the magnitude of overshoot, undershoot and settling time as a function of input rise (fall) times.

8 References

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