

Evaluation of i_{DD}/v_{OUT} Cross-Correlation for Mixed Current/Voltage Testing of Analogue and Mixed-Signal Circuits

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Abstract

The use of cross-correlation between power supply current and output voltage dynamic responses is presented as a methodology for improved mixed current /voltage testing of analogue and mixed-signal circuits. Results obtained from simulations are presented which show that better fault coverage and a simplification of test circuitry can be obtained, when compared with the results obtained from the direct observation of the individual signals. These advantages are important factors to develop viable new design for testability and built-in self test techniques.

1 Introduction

For the manufacturers of electronics products getting a product to market earlier than the competition can lead to higher profits over the product life time. Together with a reduction in throughput time in production, manufacturers are committed to improve products quality and reliability levels.

Mixed-signal circuits can be divided into two broad categories which can be identified as Register Controlled Analogue and Digitised Analogue (Fig. 1). While in the first case signal processing operations are mainly analogue and some logic is added for control and digital interfacing, in the second one the majority of signal processing is digital. Both cases, whether implemented on ICs (Integrated Circuits) or PCBs (Printed Circuit Boards), are characterised by a diversity of internal functional blocks, operating frequencies, waveforms and amplitudes. Furthermore, they have tolerance bands that are sometimes difficult to evaluate accurately, which may lead to testing errors due to imprecisely defined acceptability margins.

Different functional blocks require different test methods and more powerful test facilities capable of supporting different test methodologies and measurements, either built in circuit or in ATE (Automatic Test Equipment). Re-usability of tests that are specific for certain sub-circuits, regardless of the designs in which they are used, is a major requirement for reaching high levels of functionality, integration and modularity in mixed-signal design [1]. These problems

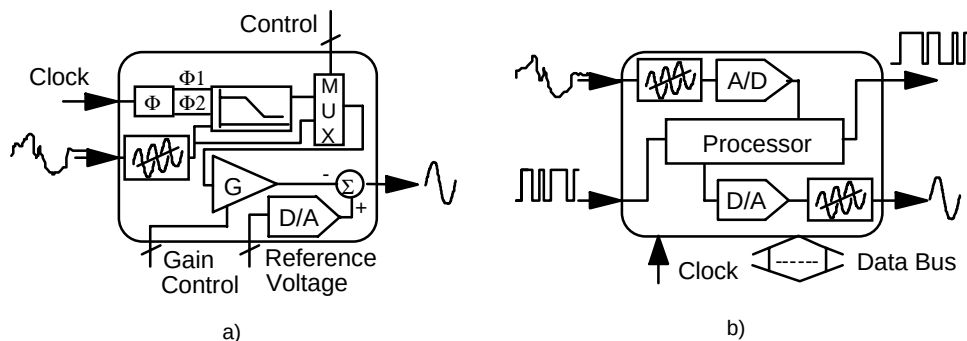


Figure 1 - Categories of mixed-signal circuits. a) Register Controlled Analogue, b) Digitised Analogue.

are even more acute for the development of BIST (Built-In Self Test) techniques as the amount of additional circuitry required may jeopardise the feasibility of any proposed BIST technique.

The extra circuitry introduced by DfT (Design for Testability) and BIST schemes is not always well accepted by manufacturing managers due to the area and cost overhead which they may represent. However, this situation is changing as the advantages of improved testability are recognised. A quality improvement factor rather than a simply overhead estimation, tends to be used as a figure of merit to qualify testing schemes [2]. The drawbacks represented by degradation of the functional behaviour of the circuits and the overhead in cost and complexity tend to be overcome by the actual benefits in quality improvement. In order to maximise this factor the ratio $efficiency/(cost*complexity)$ represented by a specific test infrastructure has to be maximised. This can be achieved by using the same test resources for a number of different purposes and by improving the test methodologies employed.

Here power supply current monitoring comes as a promising technique for the development of new test methodologies. Results published so far show that fault coverages in the order of 90% to 100% are obtainable, including the detection of faults not detectable by the output voltage, both for MOS and bipolar technologies [3 - 7].

The acceptance or rejection of a circuit under test, is required to be reliable. Testing errors like rejecting a circuit actually good or accepting one really faulty should not occur. Considering normal distribution curves for faulty responses, that is the case for parametric faults, the probability of occurrence of testing errors depends on the size of the areas defined by the overlap of fault free and faulty $f1$ distribution curves (Fig. 2).

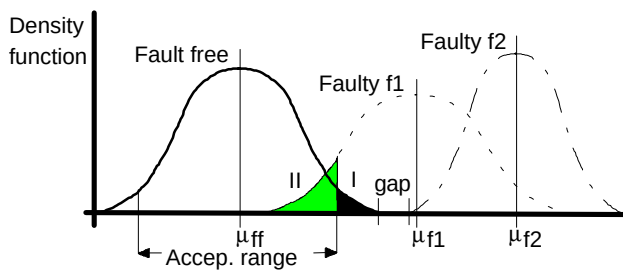


Figure 2 - Graphical representation of the fault free and faulty amplitude distribution curves.

For a certain acceptance range, the probability of a Type I error — a good device being rejected as faulty — is determined by the size of area I. Area II determines the probability of a Type II error — a faulty device being

accepted as good. In the ideal case a gap should always exist between fault free and faulty responses. Using the concept of hypothesis testing, the Z statistic equation

$$Z = \frac{(\bar{X} - \mu)}{\sigma / \sqrt{n}}$$

shows that, for a particular

distribution curve, the higher the value of σ the higher the probability of having estimated average values ($\bar{X}$), for the difference between fault-free and faulty behaviours, different from the actual average (μ). This is critical if lower as the probability of testing errors increases. It should be kept in mind that the variance of an uncertainty band due to noise and measuring errors would be added to the variance of the response deviations.

In [6] it is shown that observing both i_{DD} and output voltage (v_{OUT}) dynamic responses increases FC (Fault Coverage) levels, and allows for an improvement in test efficiency as the probability of test escapes is reduced. It was concluded that while in general i_{DD} presents better fault coverages, cases can be found where observing v_{OUT} allows to detect faults not detected by i_{DD} . An improvement on test confidence can also be obtained as often, for faults detected by both i_{DD} and v_{OUT} , one of the signals presents higher average values and smaller dispersions for the estimated faulty response deviations than the other.

In this paper the use of the cross-correlation function between i_{DD} and v_{OUT} signals is evaluated as a methodology for mixed current/voltage testing. After this introduction a theoretical background for the application of cross-correlation for mixed current/voltage testing is presented. Section 3 presents results obtained by simulation for a LPF (Low-Pass Filter) and a PLL (Phase-Locked Loop). In the fourth section the effects of the measurement quality over the effectiveness of the proposed methodology are evaluated, as well as the eventual implementation of polarised cross-correlation. Section 5 highlights the final conclusions.

2 Cross-correlation for mixed current/voltage testing

The use of correlation functions has been widely explored for dynamic testing of linear circuits and systems. Usually an input-output cross-correlation is performed as a means to find an approximate impulse response of the circuit under test [7-10]. In [7] FC results for the go/no-go testing of a mixed-signal circuit are presented which were obtained by performing the auto-correlation of the v_{OUT} response, and the cross-correlation between v_{OUT} and the input test stimulus. The good discrimination capabilities of the correlation functions allow their use for fault diagnosis purposes as well [8, 9].

The use of cross-correlation for mixed current/voltage testing was proposed in [11]. Cross-correlating i_{DD} and v_{OUT} signals allows for their processing in a single operation. One mixed current/voltage test is performed instead of two separate tests, leading to a reduction of testing time. Considering $v_{OUT}^G(t)$ and $i_{DD}^G(t)$ as the golden responses, and $v_{OUT}^F(t) = v_{OUT}^G(t) + \partial v_{OUT}(t)$ and $i_{DD}^F(t) = i_{DD}^G(t) + \partial i_{DD}(t)$ as their respective faulty responses, the cross-correlation between $v_{OUT}^F(t)$ and $i_{DD}^F(t)$ gives:

$$\begin{aligned} Rv_{OUT}^F i_{DD}^F(\tau) &= \frac{1}{T} \int_0^T v_{OUT}^F(t) \times i_{DD}^F(t + \tau) dt \\ &= \frac{1}{T} \int_0^T (v_{OUT}^G(t) + \partial v_{OUT}(t)) (i_{DD}^G(t + \tau) + \partial i_{DD}(t + \tau)) dt = \\ &= Rv_{OUT}^G i_{DD}^G(\tau) + Rv_{OUT}^G \partial i_{DD}(\tau) + \\ &+ R\partial v_{OUT} i_{DD}^G(\tau) + R\partial v_{OUT} \partial i_{DD}(\tau). \end{aligned} \quad (1)$$

From (1) it is seen that the faulty cross-correlation comprises, in a single function, three components depending of the deviations of both $v_{OUT}(t)$ and $i_{DD}(t)$, which add to the reference cross-correlation function found from the golden signals $Rv_{OUT}^G i_{DD}^G(\tau)$.

3 Results

The $v_{OUT}(t)$ and $i_{DD}(t)$ responses of a LPF and a PLL were obtained by simulation for faults in the MOS transistors (catastrophic and gate-oxide shorts), and in the passive components. A pseudo-random sequence of discrete levels and a constant frequency square-wave were used as test stimuli, respectively for the LPF and the PLL. Tolerance bands for each signals golden responses were found from Monte Carlo simulations, considering $\pm 5\%$ deviations in the passive components values and in the following typical MOS process parameters of the transistors [12]: threshold voltage, intrinsic transconductance, gate oxide thickness, metallurgical junction depth, drain and source diffusion sheet resistances, and device width and length. The distributions of the faulty responses due to acceptable parameter deviations were not evaluated in order to restrict the amount of data to be processed.

Fault detectability analysis were performed by comparing the individual $v_{OUT}(t)$ and $i_{DD}(t)$ waveforms and the cross-correlation functions with the respective golden curves. In both cases the fault detectability procedure is based on the detection of errors, i.e., deviations whose amplitude is higher than the tolerance band amplitude. A fault is considered detected if the Normalised Error Area (NEA) is $> 5\%$. NEA is given by (2) where m is the number of detected errors, and e_j and d_i the amplitudes of, respectively, error j and deviation i .

$$NEA = \frac{m \times \sum_{j=1}^m |e_j|}{n \times \sum_{i=1}^n |d_i|} \times 100\% \quad (2)$$

The threshold value of NEA establishes the maximum out-of-tolerance portion of the response, both in number of occurrences and amplitude, which is not considered as a faulty response. This allows for filtering spurious transients and small response deviations.

It is seen from the results presented in Fig. 3 that observing both $v_{OUT}(t)$ and $i_{DD}(t)$ signals allows to increase FC, and that applying cross-correlation between them allows improving it even more.

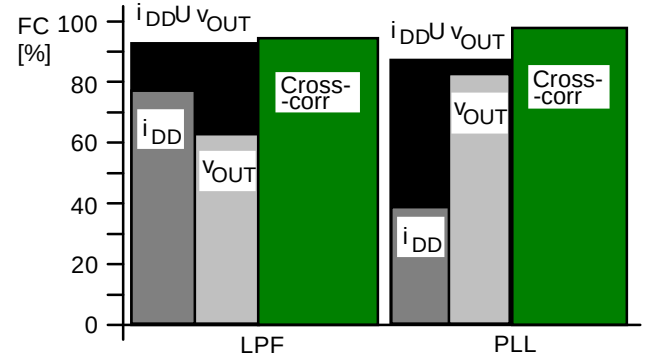


Figure 3 - Fault coverages obtained from the observation of the individual waveforms and by applying cross-correlation.

4 Effects of measurement resolution

Nevertheless, the feasibility of any testing technique depends on the circuitry required for its implementation, whether it be built in the circuit or in a test system. Having in mind the necessity for A/D (analogue to digital) conversion we find as possible limiting factors, the sampling ratio and the amplitude quantisation levels necessary to acquire the signals. Another limiting factor concerns the time delay length τ (or no. of samples in the discrete case) required to compute the cross-correlation. The smaller the values required for these parameters the better, providing the required effectiveness is guaranteed, as they determine the cost and complexity of the technique as a viable test methodology.

Concerning the implementation of this technique at board level one has to consider the infrastructures available for testing. The specification and standardisation process of a mixed-signal test bus — IEEE P1149.4 — is now in progress. Full compatibility with boundary-scan IEEE/ANSI Std. 1149.1 is mandatory to reduce investments and allow for the use of the same protocol

to control analogue and digital test functions. However, it is likely that ICs not comprising these facilities will still be used for long, and that often boards will include analogue clusters not accessible by this bus or that the low analogue content in a board will not justify the inclusion of such infrastructure.

The scheme presented in [13] proposes the inclusion of TSICs (Test Support Integrated Circuits) to provide the interface between a standard digital boundary-scan bus and analogue test nodes. Considering their use to acquire i_{DD} and v_{OUT} signals one obvious limitation comes up from the same BS chain being used to serially shift samples of both signals, leading to a division of the maximum obtainable sampling rate by the two signals. The sampling ratio is also affected by the length of the samples, i. e., the no. of bits of the A/D converter.

Fig. 4 shows the evolution of the fault coverage in both circuits for increasing values of the correlation sample delay length used in the calculations, and for varying sampling intervals and number of quantisation bits. It is seen that the FC only suffers significant reductions for

large fidelity degradations of the waveforms and that small sample delays can be used for the calculation of the cross-correlations. The FC valleys in Fig. 4-b) occur for sampling intervals coherent with the period of the PLL response waveforms. It is interesting to note the low degradation of FC with the reduction of the no. of quantisation bits. No reduction is seen in the case of the PLL because several cycles of the waveforms are used providing more response information.

The use of polarised cross-correlation, which allows to simplify the implementation of digital correlators [10], has also been investigated. In this case the signals are quantised into two logic levels (0 and 1). Results for both circuits are presented in Fig. 5, which include partial results for each type of faults. The highest reduction occurs for the GOS in the PLL. The majority of the catastrophic faults (the most likely faults to occur [4]) are still detected. These reductions are mainly due to the signals quantisation to zero, leading a significant portion of information to be lost in the multiplications to calculate the correlation functions.

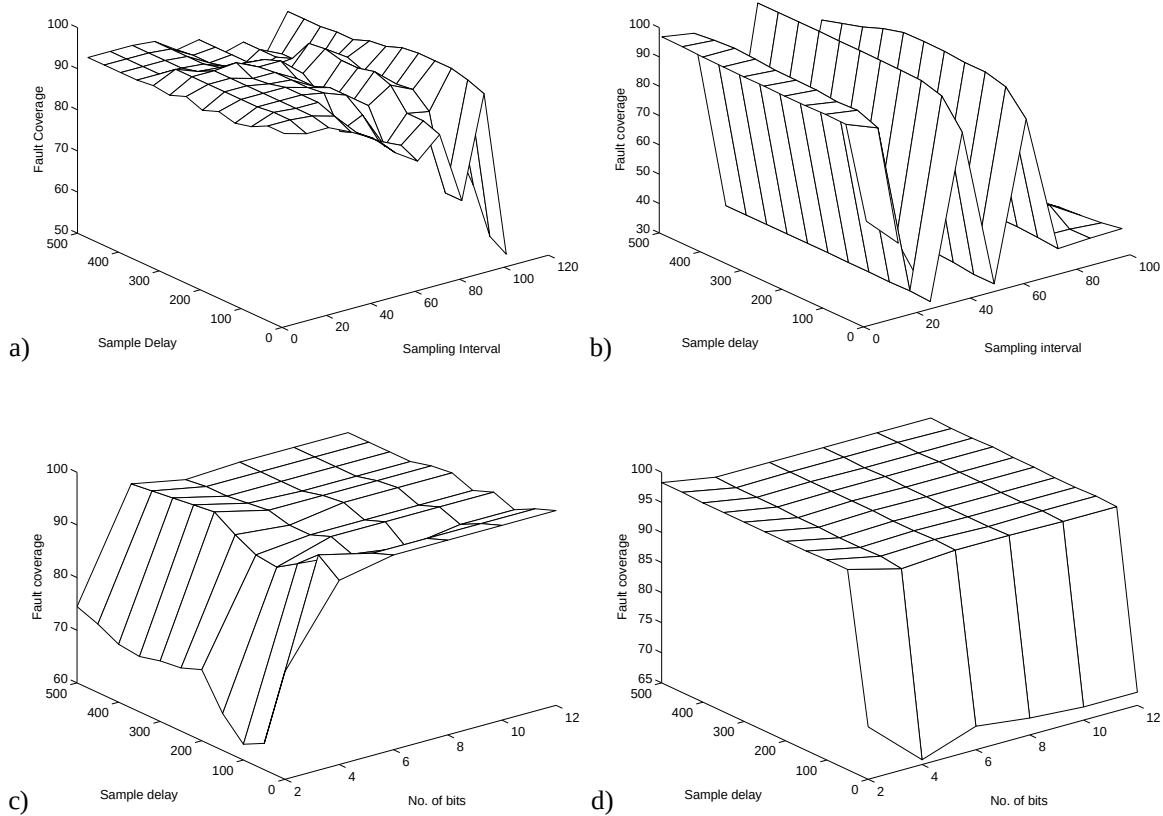


Figure 4 - Evolution of FC as a function of the correlation sample length, sampling ratio, and of quantisation level, respectively in the LPF [a), b)] and in the PLL [c), d)].

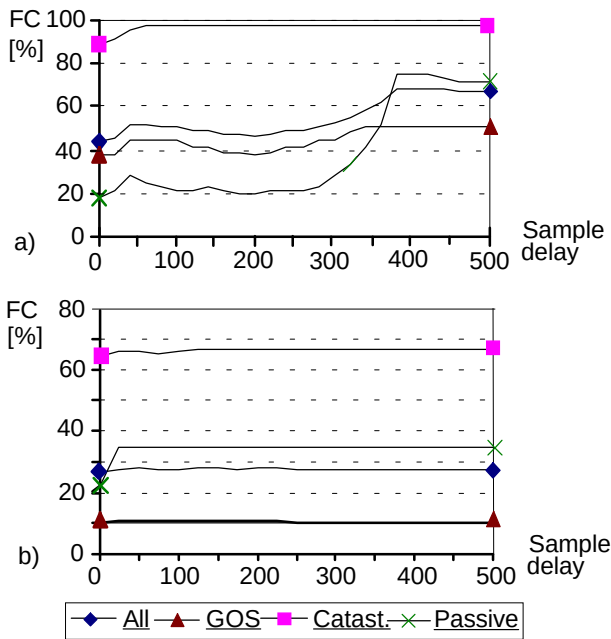


Figure 5 - Fault coverage using polarised cross-correlation for varying sample delay length: a) LPF; b) PLL.

5 Conclusions

The cross-correlation between power supply current and output voltage is evaluated as a methodology for mixed current/voltage testing of analogue and mixed-signal circuits. In this paper it is shown that testing techniques based on the observation of both power supply current and output voltage can lead to an increase in fault coverage and test efficiency, providing benefits in the final product's quality and reliability. For this purpose the cross-correlation between these signals is used as a means to process test responses in a single operation. Its implementation for testing boards making use of a digital boundary scan infrastructure is being investigated. Results obtained from the simulation of two circuits show that this technique allows for the simplification of test circuitry, making DfT and BIST schemes more affordable and more efficient.

Acknowledgements

The authors are thankful to Gaynor E. Taylor and Ian M. Bell for valuable comments. The support of *Junta Nacional de Investigação Científica e Tecnológica*,

Conselho de Reitores das Universidades Portuguesas, and British Council is also gratefully acknowledged.

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