Dongwan Shin

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Citizenship: Republic of Korea (South Korea)
Vista status: J-1 visa

Objective

Research and development of embedded computer systems and systems-on-chips (SoCs). Research on system-level design automation, high-level synthesis and low power design.

Education

06/2004 **Ph.D., Information and Computer Science**,
University of California, Irvine, CA, USA
Thesis title: *Communication Synthesis for System on Chip*
Advisor: Prof. Daniel D. Gajski

02/1997 **M.S., Electronic Engineering**,
Seoul National University, Seoul, South Korea
Thesis title: *Low power high-level synthesis by minimizing switched capacitances*
Advisor: Prof. Kiyoung Choi

02/1995 **B.S., Electronic Engineering**,
Hanyang University, Seoul, South Korea

Experience

06/2004 – Present **Project Scientist** — University of California
Center for Embedded Computer Systems — Irvine, CA

- Developing and implementing of electronic design automation tools under contract with the Japanese Aerospace Exploration Agency (JAXA).
- Developing and implementing Communication synthesis for SoC design environment.
- Supervised and led research and development team of students and developers.

04/2001 – 05/2004 **Graduate Research Assistant** — University of California
Center for Embedded Computer Systems — Irvine, CA

- Developed and implemented Communication Synthesis for SoC design environment.
- Developed and implemented RTL Synthesis for SCE.
- Researched system-level design models and methodology for contracts with Semiconductor Research Cooperation (SRC).

09/2000 – 03/2001 **Tutor** — University of California
Information and Computer Science — Irvine, CA

- Designed and graded exams and guided projects for undergraduate Operating System class.
- Graded exams for undergraduate class in Computer System Architecture class

01/2000 – 09/2000	**Part-time Research Assistant** Design Automation Lab. in Dept. of Electronic Engineering	Seoul Nation University Seoul, South Korea

- Developed power-conscious loop optimization technique in high-level synthesis
- Developed interconnect-aware high-level synthesis

09/2000 – 07/1999	**Public service of personnel** The Office of Environmental Business	Kwachon, Kyungki, South Korea

- Mandatory military service in South Korea

01/1997 – 05/1999	**Research Engineer** Design Methodology Team in System Business Unit	Hynix Semiconductor Seoul, South Korea

- Set up the ASIC design flow for LGS ASIC libraries
- Evaluated synthesis, simulation and DFT tools from various vendors
- Developed design methodology for SoCs.

03/1995 – 02/1997	**Research Assistant** Design Automation Lab. in Dept. of Electronics Engineering	Seoul Nation University Seoul, South Korea

- Developed power-conscious scheduling technique in high-level synthesis
- Designed IEEE 754 compatible floating point SRT divider with self timed ring structure
- Developed waveform viewer with MOTIF library in X-window system

03/1995 – 06/1995	**Teaching Assistant** Dept. of s Engineering	Seoul Nation University Seoul, South Korea

- Developed and guided undergraduate lab projects for microprocessor system design.

Honors and Awards

1996	Bronze Award in 2nd Chip Design Contest with *"Self-timed divider with radix-2 RSD number system"*	The Federation of Korean Industry, South Korea

Professional Service

Volunteer Activities
- Vice president of Korean Graduate Student Association in University of California, Irvine, 2003

Paper reviews
- Conferences: DAC, DATE, CODE+ISSS, ASP-DAC
- Journals: IEEE TCAD, IEEE TVLSI, ACM ToDAE, Journal of Systems and Software

Memberships
- IEEE (since 2000): Circuits & Systems Society

Tutorials and Presentations

Invited Talks
- "Embedded System Design Environment (ESE)", System Design Group, Dept. of Electrical Engineering, Seoul Nation Univ., Seoul, South Korea, November 2006
- "System-on-Chip Design Environment (SCE): Tutorial", BIT Engineering Lab., Information and Communication Univ., Daejon, South Korea, January 2006

- "Layer-based Communication Design for Automatic Generation of System-On-Chip", College of Information & Communications, Hanyang Univ., Seoul, South Korea, January 2006
- "Refinement-based System Communication Design", Dept. of Electrical Engineering, KAIST, Daejon, South Korea, October 2004
- "Refinement-based System Communication Design", Embedded System Research Center, Seoul National University, Seoul, South Korea, October 2004.
- "System-level Design for System-on-Chip", Research Institute of Information Display, Hanyang University, Seoul, South Korea, October 2004.
- "System-Level Design Language, Methodology and Environment", Embedded System Research Center, Seoul National University, Seoul, South Korea, September 2001.

Selected Publications

Book Chapter

B2. D. Shin, A. Gerstlauer, R. Dömer and D. Gajski, "An Interactive Design Environment for C-Based High-Level Synthesis," In Embedded System Design: Topics, Techniques and Trends, Editors Retteberg et al., Springer, May. 2007.

B1. D. Shin, A. Gerstlauer, R. Dömer and D. Gajski, "Automatic Generation of Communication Architectures," In From Specification to Embedded Systems Application, Editors Retteberg et al., Springer, Aug. 2005.

Journal Papers

J4. R. Dömer, A Gerstlauer, J. Peng, D. Shin, L. Cai, H. Yu, S. Abdi and D. Gajski, "System-on-Chip Environment: A SpecC-based Framework for Heterogeneous MPSoC Design," submitted to EUROASIP Journal on Embedded Systems.

J3. D. Shin, A Gerstlauer, R. Dömer and D. Gajski, "An Interactive Design Environment for C-Based High-Level Synthesis of RTL Processors," to appear in IEEE Transaction on Very Large Scale Integration Systems.

J2. A Gerstlauer, D. Shin, J. Peng, R. Dömer and D. Gajski, "Systematic, Layer-based Generation of System-On-Chip Bus Networks," IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems, Vol. 26, Issue 9, September 2007.

J1. D. Kim, D. Shin and K. Choi, "Pipelining with Common Operands for Power-Efficient Linear Systems," IEEE Transaction on Very Large Scale Integration Systems, Vol. 13, Issue 9, September 2005.

Conference Papers

C10. R. Dömer, A. Gerstlauer and D. Shin, "Cycle-accurate RTL Modeling with Multi-cycled and Pipelined Components," Proceedings of International SOC Design Conference, October 2006.

C9. D. Shin, A. Gerstlauer, Junyu Peng, R. Dömer and D. Gajski, "Automatic Generation of Transaction-level Models for Rapid Design Space Exploration," Proceedings of International Conference on Hardware/Software Codesign and System Synthesis, October 2006 (46/183 = 25.0 % acceptance rate).

C8. D. Shin, A. Gerstlauer, R. Dömer and D. Gajski, "Automatic Network Generation for System-on-Chip Communication Design," Proceedings of International Conference on Hardware/Software Codesign and System Synthesis, September 2005 (50/200 = 25.0 % acceptance rate).

C7. A. Gerstlauer, D. Shin, R. Dömer and D. Gajski, "System-Level Communication Modeling for Network-on-Chip Synthesis," Proceedings of Asia and South Pacific Design Automation Conference, January 2005 (280/692 = 40.4 % acceptance rate).

C6. D. Shin, S. Abdi and D. Gajski, “Automatic Generation of Bus Functional Models from Transaction Level Models,” Proceedings of Asia and South Pacific Design Automation Conference, January 2004 (148/291 = 50.8 % acceptance rate).

C5. S. Abdi, D. Shin and D. Gajski, “Automatic Communication Refinement for System-level Design,” Proceedings of Design Automation Conference, June 2003 (152/600 = 24.2 % acceptance rate).

C4. D. Kim, D. Shin, and K. Choi**, “**Low Power Pipelining of Linear Systems: A Common Operand Centric Approach,” Proceedings of International Symposium on Low Power Electronics and Designs, August 2001 (47/194 = 24.2 % acceptance rate).

C3. J. Jeon, D. Kim, D. Shin, and K. Choi, “High-level Synthesis under Multi-cycle Interconnect Delay,” Proceedings of Asia and South Pacific Design Automation Conference, February 2001 (83/161 = 51.5 % acceptance rate).

C2. D. Shin and K. Choi, “Low Power High Level Synthesis by Increasing Data Correlation,” Proceedings of International Symposium on Low Power Electronics and Designs, August 1997.

C1. K-J Lee, D. Shin, and K. Choi, “A Novel Self-timed Ring Structure for SRT Division,” Proceedings of International Technical Conference on Circuits, Systems, Computers and Communications, July 1996 (no acceptance rate available).

Technical Reports

R17. A. Gerstlauer, G. Schirner, D. Shin, R. Doemer, D. Gajski, “System-On-Chip Component Models,” Technical Report CECS-06-10, CECS, UC Irvine, May 2006.

R16. A. Gerstlauer, G. Schirner, D. Shin, and J. Peng, "Necessary and sufficient functionality and parameters for SoC communication," Technical Report CECS-06-01, CECS, UC Irvine, May 2006.

R15. D. Gajski, A. Gerstlauer, R. Doemer, S. Abdi, J. Peng, and D. Shin, "TL Environment," Technical Report CECS-05-10, CECS, UC Irvine, July 2005.

R14. D. Shin, A. Gerstlauer, R. Doemer and D. Gajski, “System-on-Chip Communication Modeling Style Guide,” Technical Report CECS-04-25, CECS, UC Irvine, July 2004.

R13. D. Shin, L. Cai, A. Gerstlauer, R. Doemer and D. Gajski, “System-on-Chip Transaction-level Modeling Style Guide,” Technical Report CECS-04-24, CECS, UC Irvine, July 2004.

R12. D. Shin, J. Peng, A. Gerstlauer, R. Doemer and D. Gajski, “System-on-Chip Network Modeling Style Guide,” Technical Report CECS-04-23, CECS, UC Irvine, July 2004.

R11. R. Doemer, A. Gerstlauer, and D. Shin, “Cycle-accurate RTL Modeling with Multi-Cycled and Pipelined Components,” Technical Report CECS-04-19, CECS, UC Irvine, July 22 2004.

R10. D. Shin, A. Gerstlauer, and D. Gajski, “Communication Link Synthesis for SoC,” Technical Report CECS-04-16, CECS, UC Irvine, June 10, 2004.

R9. D. Shin, A. Gerstlauer, and D. Gajski, “Network Synthesis for SoC,” Technical Report CECS-04-15, CECS, UC Irvine, June 10, 2004.

R8. D. Shin, A. Gerstlauer, R. Doemer, and D. Gajski, “C-based interactive RTL design methodology,” Technical Report CECS-03-42, CECS, UC Irvine, January 2004.

R7. S. Abdi, J. Peng, H. Yu, D. Shin, A. Gerstlauer, R. Doemer, and D. Gajski, “System-On-Chip Environment (SCE Version 2.2.0 Beta): Tutorial,” Technical Report CECS-03-27, CECS, UC Irvine, August 2003.

R6. A. Gerstlauer, L. Cai, D. Shin, R. Doemer, D. Gajski, “System-On-Chip Component Models,” Technical Report CECS-03-26, CECS, UC Irvine, August 2003.

R5. D. Gajski, J. Peng, A. Gerstlauer, H. Yu and D. Shin, “System Design Methodology and Tools,” Technical Report CECS-03-02, CECS, UC Irvine, January 2003.

R4. S. Abdi, J. Peng, R. Dömer, D. Shin, A. Gerslauer, A. Gluhak, L. Cai, Q. Xie, H. Yu, P. Zhang, and D. Gajski, “System-on-Chip Environment (SCE) Tutorial,” Technical Report CECS-02-28, CECS, UC Irvine, September 2002.

R3. D. Shin, and D. Gajski, "Interface synthesis from protocol specification," Technical Report CECS-02-13, CECS, UC Irvine, April 2002.

R2. D. Shin, and D. Gajski, "Scheduling in RTL design methodology," Technical Report ICS-01-65, ICS, UC Irvine, July 2001.

R1. P. Zhang, D. Shin, H. Yu, Q. Xie, and D. Gajski, "SpecC RTL design methodology," Technical Report ICS-00-44, ICS, UC Irvine, December 2000.

Skills

Languages
- Korean: native
- English: fluent

Computing
- Programming languages: C/C++, Java, Tcl, Perl, Python.
- System administration: Unix (Solaris, Linux), Windows (98, NT, 2000, XP).
- Web programming: HTML.

EDA/CAD
- Languages: VHDL, Verilog HDL, SystemC, SpecC.
- Tools: Synopsys (BC, DC, VCS, VSS, PrimeTime), Cadence (NC Verilog, BuildGate), SPICE/HSPICE.

Reference

Available upon request